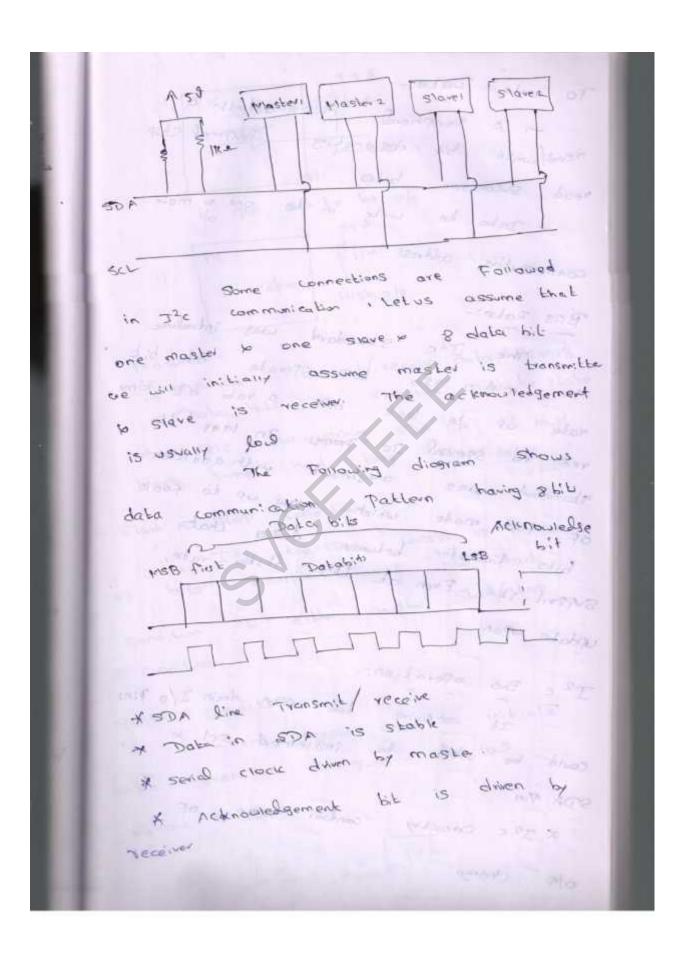
unit-III PeriPherals & InterFacing I2c Bus For Peripheral chip Access. J2c stands For Inter - integrated Circuit bus, develop by Philips som conductu I've provide 2 miles bi directional interface to a voviety of chips that Can serve as powerFul adjust to a pic TE can also serve of means for connect a moster P3, to one × A dual 8 bit, d'sital to analog X A q bit Eamp sense X A 128 6.6 Service FPROM KPC4/SD3/SDA X Re3/sck/scL Reason For open drain connection is the data transfer is bidirection p Isc par any of devices connect Can drive data line SDA Multi master multi stave connection: -A typical I2c bus showed Connection of multi-master multi-star Configuration is shown 619.



To write Data:-A peripheral chip address a Pergrand Chip bit doignating read wite successive bytes read Data to write in to mor one 101 conservutive address Rale: -Bas introduce way standard J2c The Lo operate 1980 in mid time 2/11 a vote at bits . look In 1995 rate up 20 process. rea no special JC with addition -Standard was augmen allow up to took which 24/182 Fost mode Lhat devices OF between bits transfer rate, Jaster LK:5 Even al Support 11. update upon o Pera Lion BS drain I/o Pins open YC. Quive Tt sch implement could be used to SOA AR * J2c cincuity control sige of. ole charge.

do Comican DIG Lowop set to be OP 0.47 10 453 PIC 1113h 0 19 data bits msB Tealmest -Transmit receive be stabe SDA live ADD Pitz ou Dala il must Cire when pic master driving SDA Specifica Lion hold Lime Same meet condition: SLOP consist of number start p transfel 120 blog start Stared Ligitor Stat/stop bite 30 another eithe Condition \$ conditio condition initiate START master want to when SDA 100 Puls transfer 16 data by sch. Follow 112-2 0' 50A 1 10

Prob cool :-Dala communication J2c communication both to bit stave address are Possible mbde 128 Shue address bit 1 20 inter Faced. 1.10 Can be bit Addressib mode shart, condition the address mas 501 < 3 n á a deters Sateroal Z 0 б See 1:0

ACT GE C be 63 has data deilie SIGVE 38 10 add Pecific Follos S ast as . Se \s 30 dge Slave hessed The 9.00 lo 27.0 Ac 01 E Data rea address critt Date 1 1.2 8 3 Severa 2353 50 20 Data 2040 10 in S Lat OT OT ě Por sol in beind House さんじ address , N 3 10 5 1010 Kang Internal P(B=0 General 3 a Perigrance addre 0 - hil Sead 5 P.V.O.Y

SOFT wave for J2 c communation The data transfor in J2c mode is not automatically control by hardware unlike UNRT- The mostary suitable softwa has to be granam by to generate start/stop condition various data bits from sond/receive a cknowledge m required bit of TRIIM bit bor status, RPO:setting b & recuired bit - s Sonovies dependion used for inducit Chand he taken to FS.R 'S when subroutine is address, care exten restore FSP volue complete to show on rolum. I2c Bus submodines: The Sch. Pin must have an open drain offer while SDA pin must be either on iffer or have an open drain ofp bor status, RPO:-Then charsity TRISC Finally revertion back to bank ().

SCL EAU 3 Caru 4 SDA Par INDE 'SDY of TSR naises condition two This. J2c subroulin Q,vR It these execute from main live budken no expand delay more freek, Treak, fres 20 IF free = 4 Fin (nop) , Trea 4 end if IF Fred Fill (nop) Tred 10 end is. IF Fred = 20 Fill (nop), fred Qo) end if mond mono defention milli (a) macro to variable need The equales 22 subvoutires are listed - Jont DEVADO is selected pair held ch'n address INTROD is sevented a

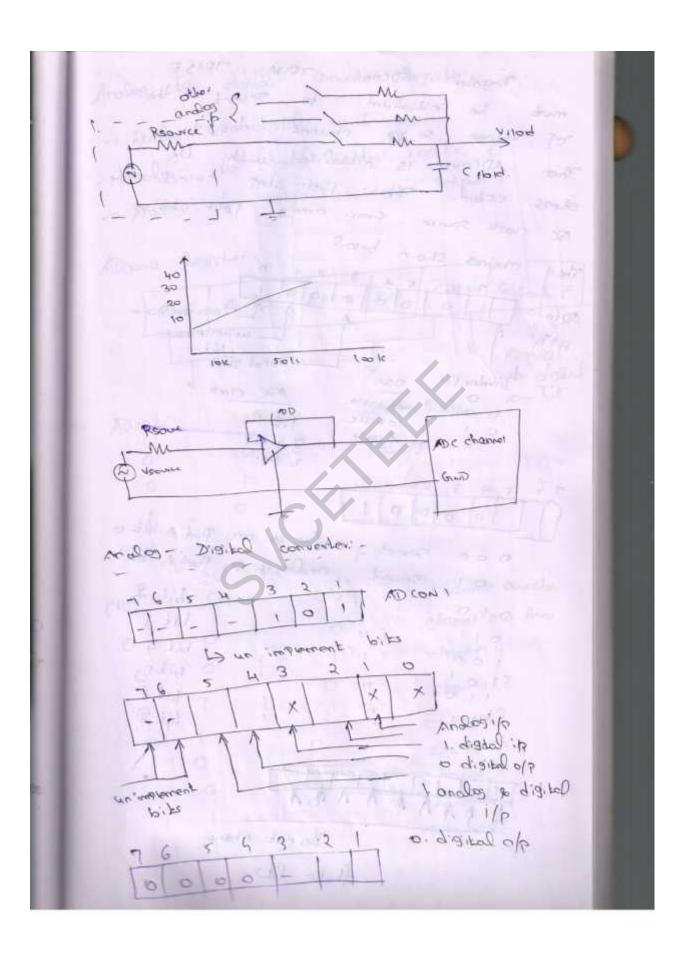
START SLOP SDA Ł stopstan > < SLOW Estan ocs symple osc = lomliz Constraint Pavametai 3 >0.645 Estart 201145 Esela Yo, Ghs F High ZONS FHORD 21 1200 LSLOP 1.36 /3 Estopsion EE PROMInon voltative storage IF controller Pic to Variable Variable 70 27 ante that instrument, device 01 there vernain 12.23 EEbou will Store d two off even arthe power

TEMP 28 18 sensal EEPRON 02, 050 0.14F ADI VCC 1050 SDA get w 2 25 internal makes use of an EEPron second during Set tod pointer Stirl message 0.299AG22 conte GL. of byte Soint bytes further 17 that. stop condition. select 10. before 10 whiteba to be data a. 4 tonow 15 Pridb address is The its Programming doing is another EEDrom Knowledge The rot acknowledge will it this autonas 80 Because command. with address conte Slave whether she k send out T SHOULD Simply check low p bit EEpron emile Pulled las by Line program +picel 1,5 with bytes mant OF glace as grapidy program as Possible 2ms, -70 Lake

b2 9 61 601 0/10/010/0 61 61 641631 content from Content 5 add Disital converter. analog to digital converter colon digital Analog signal in to Quit an Features : 8 bit Conversion channel 8 anoi 09 prolog multipleta hold circuit Siragle amping rate Adjustable citte For signal Track P De chovacheristics: pic analog to digital Cor -idealized bians tor Findlin. II 1/19 vortage to 8 bit vortage is scale e fren G asalur 1012a OV & Vilp & Viel

200 4 1450 HOH Haz 402 400 3 IR Digital Archt 319 * 12 ٩ 3 TOAN 5 GIND Connection Fig ertand Sho 01 The 10 MF 00 C. Vo 12age voltage. Y e Fevena ofop b Capacilla 30 POLION SUPPY effect orthe Suppress Pauk VDD=5y PIC 16CTX NIPPIE P 20 R 3 (of 1010 0.14 P DRT

PORT used: used Tins are For analog ip/ref. voitage Port A (Schell males S 2 Andloy PORT A PINS RAD/AND - Modeg 1/20 RAN / ANN - Modeg 1/20 RA2/AND - Modeg 1/22 RA2/AND - Modeg 1/22 RA2/AND - Modeg 1/2 / VreF RA3/AND - Modeg 1/2 / VreF RAM / Tock. - clock 1/2 Lotimero RAM / Tock. - clock 1/2 Lotimero RAM / Tock. - clock 1/2 Lotimero RAM / Tock. - Andes 1/2 H RAS/AND - Modes 1/2 H RES/AND - Modes 1/2 H RES/RD/AND - Modes 1/2 H RES/CS/ANY - MODES 1/2 LOKE & DINZ Fride fight idedized Intend ~ + 3.01 2. Pef



, TRISA, TRISE MD CON! Register to severt the witighted be kum to up channels dosined Voilage 7.9° ADCOND is initialized with the The Fast step select the Then "Fled From among - Four choices eres The clock source The choices show below 0 2 1 00 0 0 0 ine on barn 0 ADGNO unimplement HIF bit Donal star Divider For OSC ADC Clack 0 20 +1112 0 C MS 10 11112 FM1+12 US M.S. 3 < andlos ip on Put A bit o 0 10 and as you on port A bill 0 09 Select bit & 0 0 10 bit 3 0 11 bit 4 11 00 bit5 0 bitf いとう 1 1 1 Do not change these bits

Arabes to digital converter Registers. - praleg to digital result resister to chaital control register O 1 Analog register 1 digital control - Aralas 6 ADcono Register CIISO Gold CIEL Elle 2 ADOSO ADest Analog to distal on hit Clock Ral paso DOSI OSC 0 Cior? Fosc 0 0 Fosc/31 FRC Channer Number CHOO C1\$1 CIN2 channel or Ano 0 0 channel y C 0 channe 12 channel 3 0 channel h 0 0 channel 5 channelle channel7

to Digital Converter 13 Analog 000 001 010 AYD × a11 100 -00078 101 110 111 х X Analos MUNI: Prav Less FIDE Charlt Start CONF. gune NO Mode 2016 ConFigure ND in Lagt acarisition For walt 6:E =1 Stort Conversi Completion Fort Jare Tes-Read

10) Inter Facing :-Necent years LD tas been In Find wide spread use replace LED The decing Price of LO ability to deploy number - Incorporation of the Freshing Controlo - Fase of Program of characters & graphics interface to LOB Display!-PJC 00000 0 20×4 character Hite Chi Lmo444 03 Displa, TON 45.8 Rich Shir L register 154 19503 -> valid data Timiy constraints

Description TIO Interve Pin GAD VSS Serie ? +28 VDD 2 POWER SUPPLY No 3. RS =0 Rs 19 Rhs 5 R/19 = 1/0 F Enabe 6. -the Ilo 60 1/0 6. 8 110 62 P bit data 50 63 05 bit 64 0 11 8 bit data 65 7/6 12 1.12 5/0 56 13 110 57 15 LO displays Constraint For Sime Constraint Fining Pad For 20 MHZ The 121 C even Cleaved met set CON. First 15 RS STIPIF is created sel, 15 5

A more stringent timing constraint occu during initialization when a delay of atienal Juns is need blue some of . ics. Line that hitach: micro continu control codes. o Foi comy out one action Finds necessary Sendiro commands to data to LOD with devat Time +50 Ro Nec REDO VEE 8-56 VSS Roy R RWE RBO RB. RB1 LOD data Pin FOU PARAB LO_DATA Contral Phys FAN PORTB hicen RS Min OFLO Ea- 280 RB, NO PINOFLO, RS FOO BEF LOD-CIRL PORT BEOK CALL COMMUNES ; Car comail MOUMFLOD-DINIA COPY WRED to, dispiaz.