14/05/19
Ans

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 80126

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Third Semester

Electrical and Electronics Engineering

EE 8351 — DIGITAL LOGIC CIRCUITS

(Common to Electronics and Instrumentation Engineering/Instrumentation and Control Engineering)

(Regulation 2017)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert $(101.01)_2$ to decimal number.

2. Give each one example for error detecting code and error correcting code.

3. Determine the exact number of half adders and full adders required for performing the addition of two binary numbers of 5-bits length each.

4. Find the result of $A + A'D + AC'$.

5. Write down the characteristic table of JK flip-flop.

6. What is FSM? List its two basic types.

7. Define metastable state.

8. Draw the structure of PAL.

9. State the purpose of test bench.

10. Write a VHDL program for an EX-NOR gate using behavioural coding.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Design a 3-input NAND gate circuit using TTL logic. (7)

(ii) Explain in detail, the generation of Hamming code for 4-bit data. (6)

Or

(b) (i) Design a 2 input NOR gate using CMOS logic. (7)

(ii) Explain the operation of RTL inverter circuit with relevant diagrams. (6)

12. (a) (i) Design a 3 × 8 decoder using 2 × 4 decoders. Draw the truth table. (7)

(ii) Design a full adder circuit using logic gates. (6)

Or

(b) (i) Simplify and implement the logic function $F(A,B,C)=\Sigma(0,1,4,5,7)$ using logic gates. (7)

(ii) Design a 4 × 2 priority encoder using logic gates. (6)

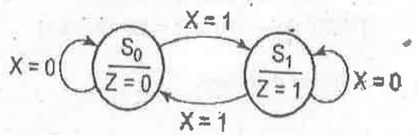
13. (a) (i) Design a 2-bit synchronous sequential down counter. (7)

(ii) Explain the operation of a 3-bit universal shift register. (6)

Or

(b) (i) Explain Moore and Mealy models with the help of block diagrams. (7)

(ii) Draw the state table for the following state diagram. (6)



14. (a) (i) Design a Modulo-6 asynchronous binary up-counter. (7)

(ii) Implement the functions $F_1(X,Y,Z)=\Sigma(1,2,4,5)$, $F_2(X,Y,Z)=\Sigma(0,1,3,4)$ and $F_3(X,Y,Z)=\Sigma(23,6,7)$ using a single PROM grid. (6)

Or

(b) (i) Differentiate PAL and PLA implementations with the help of the same example $F_2(a,b,c)=\Sigma(0,1,3,4,6,7)$. (7)

(ii) Explain the structure of CPLD with the help of a block diagram. (6)

15. (a) (i) Draw the VLSI design flow chart used for IC design and fabrication. (7)

(ii) Write down a VHDL code for 8 × 1 Demultiplexer. (6)

Or

(b) (i) Illustrate the two approaches used in VHDL coding with full adder design as your example. (7)

(ii) What are components in VHDL? Show step-by-step how a NOR gate component can be created and added in the library. (6)

PART C — (1 × 15 = 15 marks)

16. (a) Design a synchronous sequential logic circuit that goes through the sequence 0, 2, 4, 6, 8, 10, 12,14 repeatedly. Use D flip flops for your design. (15)

Or

(b) Simplify the following function and implement it using NAND gates only: $F(w,x,y,z)=\Sigma(1,3,5,7,9,11,13,15)$, with don't care states $d(w,x,y,z)=\Sigma(0,2,4,6,8)$. (15)

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10/11/2018 AN

Reg. No. :

Question Paper Code : 25084

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2018.

Third Semester

Electrical and Electronics Engineering

EE 8351 — DIGITAL LOGIC CIRCUITS

(Common to : Electronics and Instrumentation Engineering/Instrumentation and Control Engineering)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw the DTL based NAND gate.
2. Perform subtraction on the following unsigned binary numbers using the 2's-complement of the subtrahend (a) 11011 – 11001 (b) 110100 –10101
3. Mention the dependency of output in combinational circuits.
4. Draw the NAND gate circuit using NOT, AND & OR Gates.
5. Write the role of master clock generator in synchronous circuits.
6. Comment about a preset table counter & ripple counter.
7. Draw the block diagram of asynchronous sequential circuit.
8. Outline about PLA.
9. Draw the basic structure of MOS transistor.
10. List the languages that are combined together to get VHDL language.

PART B — (5 × 13 = 65 marks)

11. (a) Assume a 3-input AND gate with output F and a 3-input OR gate with G output. Show the signals of the outputs F and G as functions of the three inputs ABC. Use all 8 possible combinations of inputs ABC. (13)

Or

(b) Show that a positive logic NAND gate is a negative logic NOR gate and vice versa. (13)

12. (a) Given the following Boolean function $F = A'C + A'B + AB'C + BC$. (13)

(i) Express it in sum of minterms.

(ii) Find the minimal sum of products expression.

Or

(b) Draw the logic diagram of a 2-to-4 line decoder using NOR gates only. Include an enable input. (13)

13. (a) Explain the operation, state diagram and characteristics of a T flip-flop and master-slave JK flip-flop. (13)

Or

(b) Describe the design procedure with neat diagram about 4 bit bidirectional shift register with parallel load. (13)

14. (a) Discuss the operation of SR Latch with NOR and NAND gates analysis. (13)

Or

(b) Illustrate about hazards in sequential circuits and the steps to avoid hazards in it. (13)

15. (a) Explain the structure and working principles of TTL based Totem-pole output configuration. (13)

Or

(b) Write a VHDL code to realize a half adder using behavioral modeling and structural modeling. (13)

PART C — (1 × 15 = 15 marks)

16. (a) Design a sequential circuit with two D flip-flops A and B, and one input x. When $x = 0$, the state of the circuit remains the same. When $x = 1$, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats. (15)

Or

(b) Design a combinational circuit with three inputs, x, y and z, and the three outputs, A, B, and C. when the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input. (15)

Reg. No. :

Question Paper Code : 90194

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2019

Third Semester

Electrical and Electronics Engineering

EE 8351 – DIGITAL LOGIC CIRCUITS

Common to : Electronics and Instrumentation Engineering/Instrumentation and Control Engineering

(Regulations 2017)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A (10×2=20 Marks)

1. List the different types of output configuration in TTL.
2. Given the two binary numbers X = 1010100 and Y = 1000011, perform subtraction (a) X – Y and (b) Y – X using 2's-complements.
3. Write the difference between sequential and combinational circuits.
4. Draw basic configuration of three PLDs.
5. Mention the role of master clock generator in synchronous circuits.
6. Define state assignment.
7. Name the three types of hazards.
8. Define synchronous sequential circuit.
9. Mention the languages that are combined together to get VHDL language.
10. Expand the T'Base and T'Low predefined attributes.

PART – B **(5×13=65 Marks)**

11. a) Explain the two types of MOS families. **(13)**

(OR)

b) With the neat circuit diagram, explain the operation of ECL. **(13)**

12. a) Simplify the following expressions in (1) sum of products and (2) products of sums

a) $x'z' + y'z' + yz' + xy$ **(4)**

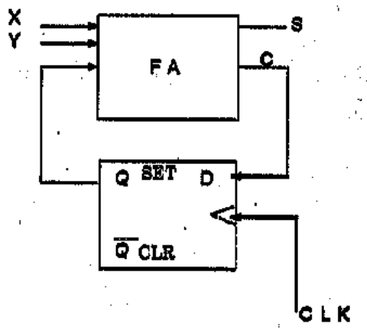
b) $AC' + B'D + A'CD + ABCD$ **(4)**

c) $(A' + B' + D')(A + B' + C')(A' + B + D')(B + C' + D')$ **(5)**

(OR)

b) Design a half subtractor circuit with inputs x and y and outputs D and B. The circuit subtracts the bits x-y and places the difference in D and the borrow in B. **(13)**

13. a) A sequential circuit has one flip-flop Q, two inputs x and y and one output S. It consists of a full-adder circuit connected to a D flip-flop, as shown in figure. Derive the state table and state diagram of the sequential circuit. **(13)**



(OR)

b) Draw and explain the operation of a JK and master slave JK flip flop. **(13)**

14. a) Discuss about the hazards in asynchronous sequential circuits and the methods to eliminate them. **(13)**

(OR)

b) Describe the effect of races in asynchronous sequential circuit design. **(13)**

15. a) Develop a VHDL code to realize a 3 bit Gray code counter using case statement. **(13)**

(OR)

b) Discuss briefly the operators and packages in VHDL. **(13)**

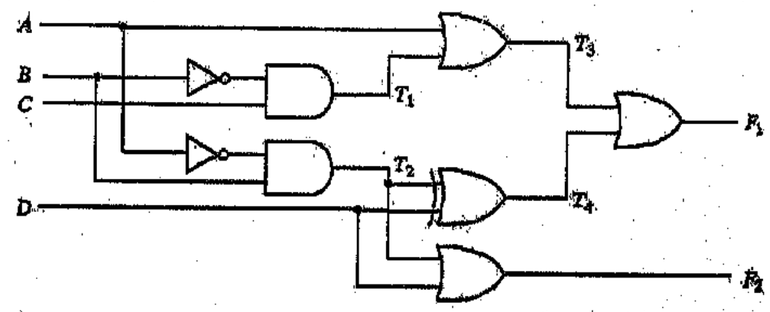
PART – C **(1×15=15 Marks)**

16. a) Consider the combinational circuit shown in Fig. **(15)**

i) Derive the Boolean expressions for T_1 through T_4. Evaluate the outputs of F_1 and F_2 as a function of the four inputs.

ii) List the truth table with 16 binary combinations of the four inputs variables. Then list the binary values for T_1 through T_4 and outputs F_1 and F_2 in the table.

iii) Plot the output Boolean functions obtained in part (b) on maps and show that the simplified Boolean expressions are equivalent to the ones obtained in part (a).



(OR)

b) Implement the following function using PLA and PAL: $F_1(A,B,C) = \Sigma m(3,5,6,7)$ and $F_2(A, B, C) = \Sigma m(0,2,4,7)$. **(15)**

Reg. No. | | | | | | | | | | | | |

Question Paper Code : 57308

01/07/16 AN

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Third Semester

Electrical and Electronics Engineering

EE 6301 – DIGITAL LOGIC CIRCUITS

(Common to Electronics and Instrumentation Engineering and Instrumentation and Control Engineering)

(Regulation 2013)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. Convert the following binary code into a Gray Code :

   1010111000_2

2. Define fan-in and fan-out.

3. Write the POS representation of the following SOP function :

   $f(x, y, z) = \sum m (0, 1, 3, 5, 7)$

4. Design a half subtractor.

5. Give the characteristic equation and characteristic table of SR flip-flop.

6. State any two differences between Moore and Mealy state machines.

7. What are the two types of asynchronous sequential circuits ?

8. State the difference between PROM, PLA and PAL.

9. What is data flow modelling in VHDL ? Give its basic mechanism.

10. Write the VHDL code to realize a 2 × 1 multiplexer.

PART – B (5 × 16 = 80 Marks)

11. (a) (i) Convert 1010111011101100_2 into its octal, decimal and hexadecimal equivalent. (6)

(ii) Deduce the odd parity hamming code for the data : 1010. Introduce an error in the LSB of the hamming code and deduce the steps to detect the error. (10)

OR

(b) (i) With circuit schematic explain the operation of a two input TTL NAND gate. (8)

(ii) With circuit schematic and explain the operation and characteristics of a ECL gate. (8)

12. (a) (i) Simplify the following function using Karnaugh Map.
$f(w, x, y, z) = \sum m(0, 1, 3, 9, 10, 12, 13, 14) + \sum d(2, 5, 6, 11)$ (8)

(ii) Implement the following function using only NAND gates :
$f(x, y, z) = \sum m(0, 2, 4, 6)$ (8)

OR

(b) (i) Design a BCD to Excess-3 code converter. (8)

(ii) Design a full adder and implement it using suitable multiplexer. (8)

13. (a) (i) Explain the operation of a JK master slave flip flop. (8)

(ii) Design a MOD-5 counter using T Flip Flops. (8)

OR

(b) (i) Design a serial adder using Mealy state model. (8)

(ii) Explain the state minimization using partitioning procedure with a suitable example. (8)

14. (a) (i) What are Static-0 and Static-1 hazards ? Explain the removal of hazards using hazard covers in K-map. (8)

(ii) Explain cycles and races in asynchronous sequential circuits. (8)

OR

(b) (i) What are transition table and flow table ? Give suitable examples. (6)

(ii) Implement the following function using PLA and PAL : (10)
$f(x, y, z) = \sum m(0, 1, 3, 5, 7)$

15. (a) (i) Explain the various operators supported by VHDL. (8)

(ii) Write the VHDL code to realize a decade counter with behavioural modelling. (8)

OR

(b) (i) Explain functions and subprograms with suitable examples. (6)

(ii) Write the VHDL code to realize a 4-bit parallel binary adder with structural modelling and write the test bench to verify its functionality. (10)

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 71764 18/05/17 AN

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2017.

Third Semester

Electrical and Electronics Engineering

EE 6301 — DIGITAL LOGIC CIRCUITS

(Common to Electronics and Instrumentation Engineering, Instrumentation and Control Engineering)

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Reduce $a(b+bc')+ab'$.

2. Convert 143_{10} into its binary and binary coded decimal equivalent.

3. Write the *POS* form of the *SOP* expression $f(x,y,z) = x'yz + xyz' + xy'z$.

4. Design a Half Subtractor.

5. Give the characteristic equation and characteristic table of a T Flip Flop.

6. State the differences between Moore and Melay state machines.

7. What is a flow table? Give example.

8. State the difference between PROM, PAL and PLA.

9. Give the syntax for package declaration and package body in VHDL.

10. Write the VHDL code for a 2 × 1 multiplexer using behavioral modeling.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Design a odd-parity hamming code generator and detector for 4-bit data and explain their logic.

(ii) Convert $FACE_{16}$ into its binary, octal and decimal equivalent.

Or

(b) (i) With circuit schematic explain the working of a two-input TTL NAND gate.

(ii) Compare Totem Pole and open collector outputs.

12. (a) (i) Reduce the following minterms using Karnaugh – Map
$f(w,x,y,z) = \sum m(0,1,3,5,6,7,8,12,14) + \sum d(9,15)$. (7)

(ii) Implement the following function using a suitable multiplexer
$f(a,b,c) = \sum m(3,7,4,5)$. (6)

Or

(b) (i) Design a 3 × 8 decoder and explain its operation as a minterm generator. (7)

(ii) Design a full adder using only NOR gates. (6)

13. (a) (i) Draw and explain the operation of a Master – Slave JK Flip Flop. (7)

(ii) Design a 5-bit ring counter and mention its applications. (6)

Or

(b) (i) Design a 4-bit parallel-in serial-out shift register using D Flip Flops. (7)

(ii) Using partitioning minimization procedure reduce the following state table : (6)

Present state	Next state		Output
	$w=0$	$w=1$	Z
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

14. (a) A control mechanism for a vending machine accepts nickels and dimes. It dispense merchandise when 20 cents is deposited ; it does not give change if 25 cents is deposited. Design the FSM that implements the required control, using as few states as possible. Find a suitable assignment and derive next-state and output expressions. (13)

Or

(b) (i) Implement the following logic and analyse for the pressure of any hazard $f = x_1x_2 + \bar{x}_1x_3$. If hazard is present briefly explain the type of hazard and design a hazard-free circuit. (7)

(ii) Implement the following functions using programmable logic array :
$f_1(x,y,z) = \sum m(0,1,3,5,7)$
$f_2(x,y,z) = \sum m(2,4,6)$. (6)

15. (a) Design a 3 –bit magnitude comparator and write the VHDL code to realize it using structural modeling. (13)

Or

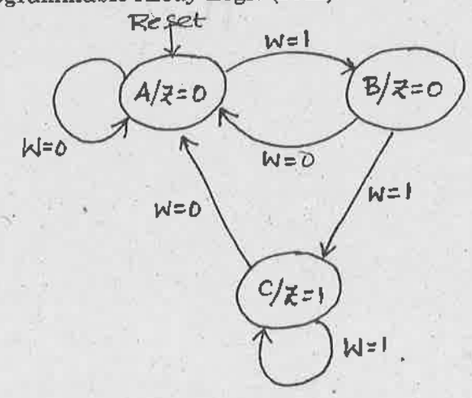
(b) Design a 4 × 4 array multiplier and write the VHDL code to realize it using structural modeling. (13)

PART C — (1 × 15 = 15 marks)

16. (a) Design a CMOS inverter and explain its operation. Comment on its characteristics such as Fan-in, Fan-out power dissipation, propagation delay and noise margin. Compare its advantages over other logic families. (15)

Or

(b) Write the VHDL code for the given state diagram, using behavioral modeling. Design it using one-hot state assignment and implement it using Programmable Array Logic (PAL). (15)



Reg. No. :

Question Paper Code : 40991

24/04/2018

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2018
Third Semester
Electrical and Electronics Engineering
EE 6301 – DIGITAL LOGIC CIRCUITS
(Common to Electronics and Instrumentation Engineering/Instrumentation and Control Engineering)
(Regulations 2013)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A (10×2=20 Marks)

1. State the associative property of Boolean algebra.
2. Reduce A(A + B).
3. Define duality property.
4. What is a karnaugh map ?
5. What is a master-slave flip-flop ?
6. Give the comparison between synchronous and asynchronous counters.
7. Define address and word.
8. Why was PAL developed ?
9. Define Cache memory.
10. Infer the concept of switch-level modeling.

PART – B (5×13=65 Marks)

11. a) i) Prove that $ABC + ABC' + AB'C + A'BC = AB + AC + BC$. (8)
ii) Convert the given expression in canonical SOP form Y = AC + AB + BC. (5)

(OR)

b) Designing a 4-bit Adder-Subtractor circuit. (13)

12. a) Write down the steps in implementing a Boolean function with levels of AND gates. (13)

(OR)

b) Give the general procedure for converting a Boolean expression in to multilevel NAND diagram. (13)

13. a) Explain the operation of SR flip-flop, T flip-flop and JK flip-flop. (13)

(OR)

b) Explain the flip-flop excitation tables for JK flip-flop and RS flip-flop. (13)

14. a) Elaborate the concept of PROM, EPROM, EEPROM in detail. (13)

(OR)

b) Explain the operation of bipolar RAM cell with suitable diagram. (13)

15. a) Give the different arithmetic operators and bitwise operators. (13)

(OR)

b) Explain in detail about the principal of operation of RTL design. (13)

PART – C (1×15=15 Marks)

16. a) Draw the circuit of CMOS AND gate and explain its operation. Also implement using PHDL. (15)

(OR)

b) Design and explain and bit shift register. Also give its truth table with its input and output waveform. (15)

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06/05/19 AN

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 52945

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Third Semester

Electrical and Electronics Engineering

EE 6301 — DIGITAL LOGIC CIRCUITS

(Common to B.E. Electronics and Instrumentation Engineering/B.E. Instrumentation and Control Engineering)

(Regulation 2013)

(Also common to: PTEE 6301 – Digital Logic circuits for B.E. (Part-Time) Third Semester – Electrical and Electronics Engineering Regulation 2014)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert a binary number $(1101101)_2$ to decimal and octal numbers.
2. Define Tri-state gates.
3. Write the logic expression for Full adder and Full subtractor.
4. What is meant by canonical form? Give an example for POS and SOP canonical forms.
5. Draw the sequential logic diagram for Parallel In — Serial Out Shift register.
6. Write the characteristic equation of JK flip flop and its truth table.
7. Define race condition. How it can be eliminated.
8. Describe PROM.
9. List the purpose of Test bench.
10. Design a Half adder using HDL

PART B — (5 × 13 = 65 marks)

11. (a) Define Binary code. Demonstrate the Hamming code with an example. (13)

Or

(b) Explain TTL logic in detail along with its types. (13)

12. (a) Design a Combinational logic circuit to convert Binary to Gray code and write its truth table. (13)

Or

(b) Implement the following Boolean function using 4:1 Multiplexer. (13)

$F(W, X, Y, Z) = \Sigma m(0, 1, 2, 4, 6, 9, 12, 14)$

13. (a) Synthesis a 3 bit counter using T Flip Flop (State diagram, Excitation table, K-map, Logic diagram). (13)

Or

(b) What is meant by a Flip Flop? Write the characteristics equation, characteristics table and draw logic of SR, JK and D flip flops. (2+4+4+3)

14. (a) Explain the steps for the design of Asynchronous sequential circuits with an example. (13)

Or

(b) Draw a PLA circuit to implement the functions (13)

$F_1 = AB' + AC + A'BC'$ and $F_2 = (AC + BC)'$.

15. (a) Describe RTL in HDL with an example.

Or

(b) (i) Write the HDL program for 2:1 multiplexer in Dataflow and Behavioral Description. (6)

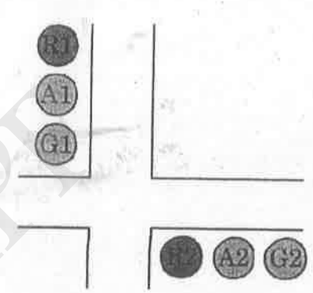
(ii) Write program in HDL to design 2 bit up/down counter. (7)

PART C — (1 × 15 = 15 marks)

16. (a) Design an asynchronous circuit that has two inputs X_1 and X_2 and one output Z. The circuit is required to give an output whenever the input sequence (0, 0) (0, 1) and (1, 1) received but only in that order. Design it using T flip flop. (15)

Or

(b) Design a synchronous digital circuit, a Moore machine, which operates this traffic light at two types of road crossing.

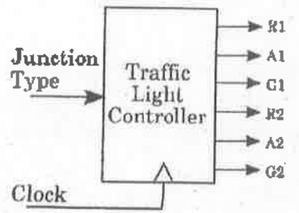


Quiet Junction

Red	Green
Red	Amber
Green	Red
Amber	Red

Busy Junction

Red	Green
Red	Amber
Red	Red
Green	Red
Amber	Red
Red	Red



Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 80366

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Third Semester

Electrical and Electronics Engineering

EE 6301 — DIGITAL LOGIC CIRCUITS

(Common to Electronics and Instrumentation Engineering and Instrumentation and Control Engineering)

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Construct OR gate and AND gate using NAND gates.
2. Convert the following Excess - 3 numbers into decimal numbers.
   (a) 1011
   (b) 1001 0011 0111
3. Convert the given expression in canonical SOP form
   Y = AB + A'C + BC'
4. Draw the truth table of 2 :1 MUX.
5. Differentiate Mealy and Moore model.
6. Draw the state diagram of JK flip flop.
7. What is static hazard and dynamic hazard?
8. Define races in asynchronous sequential circuits.
9. Write VHDL behavioral model for D flip flop.
10. Write the VHDL code for a logical gate which gives high output only when both the inputs are high.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Explain with an aid of circuit diagram the operation of 2 input CMOS NAND gate and list out its advantages over other logic families. (10)

    (ii) Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction $Y - X$ by using 2's complements. (3)

    Or

    (b) (i) Explain in detail the usage of Hamming codes for error detection and error correction with an example considering the data bits as 0101. (10)

    (ii) Convert 23.625_{10} to octal (base 8). (3)

12. (a) Simplify the logical expression using K-map in SOP and POS form $F(A,B,C,D) = \Sigma m(0, 2, 3, 6, 7) + d(8, 10, 11, 15)$. (13)

Or

(b) Design a full subtractor and realise using logic gates. Also, implement the same using half subtractors (13)

13. (a) Design a sequence detector that produces an output '1' whenever the non-overlapping sequence 101101 is detected. (13)

Or

(b) (i) Explain the realization of JK flip flop from T flip flop. (7)

(ii) Write short notes on SIPO and draw the output waveforms. (6)

14. (a) Design an asynchronous circuit that has two inputs $x1$ and $x2$ and one output z. The circuit is required to give an output whenever the input sequence (0,0), (0,1) and (1, 1) received but only in that order (13)

Or

(b) (i) Design a PLA structure using AND and OR logic for the following functions. (10)

$F1 = \Sigma m(0, 1, 2, 3, 4, 7, 8, 11, 12, 15)$

$F2 = \Sigma m(2, 3, 6, 7, 8, 9, 12, 13)$

$F3 = \Sigma m(1, 3, 7, 8, 11, 12, 15)$

$F4 = \Sigma m(0, 1, 4, 8, 11, 12, 15)$

(ii) Compare PLA and PAL circuits. (3)

15. (a) Explain in detail the concept of structural modeling in VHDL with an example of full adder. (13)

Or

(b) (i) Write short notes on built- in operators used in VHDL programming. (6)

(ii) Write VHDL coding for 4 × 1 Multiplexer. (7)

PART C — (1 × 15 = 15 marks)

16. (a) Assume that there is a parking area in a shop whose capacity is 10. No more than 10 cars are allowed inside the parking area and the gate is closed as soon as the capacity is reached. There is a gate sensor to detect the entry of car which is to be synchronized with the clock pulse. Design and implement a suitable counter using JK flip flops. Also, determine the number of flip flops to be used if the capacity is increased to 50. (15)

Or

(b) Design a 4 bit code converter which converts given binary code into a code in which the adjacent number differs by only 1 by the preceding number. Also, develop VHDL coding for the above mentioned code converter. (15)

18.11.17 FN

Reg. No. :

Question Paper Code : 50473

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2017

Third Semester

Electrical and Electronics Engineering

EE 6301 – DIGITAL LOGIC CIRCUITS

(Common to Electronics and Instrumentation Engineering/Instrumentation and Control Engineering)

(Regulations 2013)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A (10×2=20 Marks)

1. Convert $(115)_{10}$ and $(235)_{10}$ to hexadecimal numbers.
2. What is a gray code and mention its advantages.
3. What is a K-map ?
4. Compare decoder and demultiplexer.
5. What do you mean by race around condition in a flip-flop ?
6. What is a preset table counter and ripple counter ?
7. What happens to the information stored in a memory location after it has been read and write operation ?
8. What is Programmable Logic Array ?
9. Define modularity.
10. What are the languages that are combined together to get VHDL language ?

PART – B (5×13=65 Marks)

11. a) Explain in detail about error detecting and error correcting code. (13)

(OR)

b) Write short notes on following : (13)
i) RTL ii) DTL iii) TTL and iv) ECL

12. a) I) Plot the logical expression $ABCD + A\bar{B}\bar{C}\bar{D} + A\bar{B}C + AB$ on a 4-variable K-map; obtain the simplified expression from the map. (7)

II) Express the function $Y = A + \bar{B}C$ in canonical SOP and canonical POS form. (6)

(OR)

b) Design a 4-bit gray code to binary converter and express using logic gates. (13)

13. a) Explain the operation, state diagram and characteristics of T-flip-flop and master-slave JK flip-flop. (13)

(OR)

b) Explain in detail about different shift registers. (13)

14. a) Discuss about the hazards in asynchronous sequential circuit and the ways to eliminate them. (13)

(OR)

b) I) Write short notes on PLA and PAL. (7)

II) What is hazards ? Explain hazards in digital circuits. (6)

15. a) Write a VHDL code to realize a full adder using behavioural modeling and structural modeling. (13)

(OR)

b) I) Discuss briefly the packages in VHDL. (6)

II) Write an VHDL coding for realization of clocked SR flip-flop. (7)

PART – C (1×15=15 Marks)

16. a) Design an asynchronous sequential circuit with two inputs x_1 and x_2 and one output Z. Initially, both inputs are equal to zero. When x_1 or x_2 becomes 1, the output Z becomes 1. When the second input also becomes 1, the output changes to 0. The output stays at 0 until the circuit goes back to the initial state. (15)

(OR)

b) I) Design a full adder using 4 × 1 multiplexer, also write its truth table and draw the logical diagram. (8)

II) Describe level triggering and edge triggering. (7)

15/12/18

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 20447

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2018.

Third Semester

Electrical and Electronics Engineering

EE 6301 — DIGITAL LOGIC CIRCUITS

(Common to: Electronics and Instrumentation Engineering/ Instrumentation and Control Engineering)

(Regulations 2013)

(Also Common to: PTEE 6301 — Digital Logic Circuits for B.E. (Part-Time) – Third Semester – Electrical and Electronics Engineering – Regulations 2014)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert $(115)_{10}$ and $(235)_{10}$ to hexadecimal numbers.

2. Write about a gray code and mention it's advantages.

3. Define K-map.

4. Compare decoder and Demultiplexer.

5. Mention about race around condition in a flip-flop.

6. What is a presettable counter and ripple counter?

7. What happens to the information stored in a memory location after it has been read and write operation?

8. What is Programmable Logic Array?

9. Define modularity.

10. List the languages that are combined together to get VHDL language.

PART B — (5 × 13 = 65 marks)

11. (a) Explain in detail about error detecting and error correcting code. (13)

Or

(b) Write short notes on following :

(i) RTL,

(ii) DTL,

(iii) TTL and

(iv) ECL. (13)

12. (a) (i) Plot the logical expression $ABCD + A\overline{B}\,\overline{C}\,\overline{D} + A\overline{B}C + AB$ on a 4-variable K-map; obtain the simplified expression from the map. (7)

(ii) Express the function $Y = A + \overline{B}C$ in canonical SOP and canonical POS form. (6)

Or

(b) Design a 4-bit gray code to binary converter and express using logic gates. (13)

13. (a) Explain the operation, state diagram and characteristics of T flip-flop and master-slave JK flip-flop. (13)

Or

(b) Explain in detail about different shift registers. (13)

14. (a) Discuss about the hazards in asynchronous sequential circuit and the ways to eliminate them. (13)

Or

(b) Design an asynchronous circuit that will operate only for the first pulse received whenever a control input is asserted from LOW to HIGH state. Further pulses will be ignored. (13)

15. (a) Implement a full adder circuit using PLA having three inputs, eight product terms, and two outputs. (13)

Or

(b) Briefly explain the operations involved using RAM and compare Static RAM and Dynamic RAM. (13)

PART C — (1 × 15 = 15 marks)

16. (a) Design a logic circuit that has three inputs, A, B, C and whose output will be HIGH only when a majority of the inputs are HIGH. (15)

Or

(b) Apply K-map and simplify the following.

$y = \overline{C}\left(\overline{ABD} + D\right) + A\overline{B}C + \overline{D}$ (15)

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22/11/19 AN

Reg. No. :

Question Paper Code : 91480

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2019

Third Semester

Electrical and Electronics Engineering

EE 6301 – DIGITAL LOGIC CIRCUITS

(Common to Electronics and Instrumentation Engineering, Instrumentation and Control Engineering)

(Regulations 2013)

(Also common to PTEE 6301 – Digital Logic Circuits for B.E.(Part-Time) – Third Semester – Electrical and Electronics Engineering – Regulations 2014)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Reduce $a(b+bc')+ab'$.
2. Convert 143_{10} into its binary and binary coded decimal equivalent.
3. Convert the given expression in canonical SOP form

   $Y = AC + AB + BC$.
4. Simplify the expression $Z = AB + A\bar{B}\cdot\left(\overline{\bar{A}.\bar{C}}\right)$.
5. Give the characteristic equation and characteristic table of SR flip-flop.
6. State any two differences between Moore and Mealy state machines.
7. What happens to the information stored in a memory location after it has been read and write operation ?

8. What is Programmable Logic Array ?

9. Write VHDL behavioral model for D flip-flop.

10. Write the VHDL code for a logical gate which gives high output only when both the inputs are high.

PART – B (5×13=65 Marks)

11. a) i) Convert 1010111011101100_2 into its octal, decimal and hexadecimal equivalent. (6)

ii) Deduce the odd parity hamming code for the data : 1010.
Introduce an error in the LSB of the hamming code and deduce the steps to detect the error. (7)

(OR)

b) i) With circuit schematic explain the operation of a two input TTL NAND gate. (6)

ii) With circuit schematic and explain the operation and characteristics of a ECL gate. (7)

12. a) Simplify the logical expression using K-map in SOP and POS form $F(A, B, C, D) = \Sigma m\ (0, 2, 3, 6, 7) + d(8, 10, 11, 15)$. (13)

(OR)

b) Design a full subtractor and realise using logic gates. Also, implement the same using half subtractors. (13)

13. a) i) Explain the operation of a master slave JK flip-flop. (7)

ii) Design a 3-bit bidirectional shift register. (6)

(OR)

b) i) Design a MOD-5 synchronous counter using JK flip-flops. (7)

ii) Design a sequence detector to detect the sequence 101 using JK flip-flop. (6)

14. a) Design an asynchronous sequential circuit that has two inputs X_2 and X_1 and one output Z. When $X_1 = 0$, the output Z is 0. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0.

(OR)

b) i) Implement the following function using PLA : (7)
$F(x, y, z) = \Sigma m(1, 2, 4, 6)$

ii) For the given Boolean function, obtain the hazard-free circuit. (6)
$F(A, B, C, D) = \Sigma m(1, 3, 6, 7, 13, 15)$.

15. a) Write a VHDL code to realize a full adder using behavioural modeling and structural modeling. (13)

(OR)

b) i) Discuss briefly the packages in VHDL. (6)

ii) Write an VHDL coding for realization of clocked SR flip-flop. (7)

PART – C (1×15=15 Marks)

16. a) i) A sequential circuit with D flip-flops A and B, input X and Y is specified by the following next state and output equations,
$A(t + 1) = AX + BX$,
$B(t + 1) = \overline{A}X$
$Y = (A + B)\overline{X}$
Draw the logic diagram, derive state table and state diagram. (12)

ii) Realize T flip-flop using JK flip-flop. (3)

(OR)

b) i) Design a full Adder using 4 × 1 multiplexer, also write its truth table and draw the logical diagram. (10)

ii) Describe level triggering and edge triggering. (5)

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : X 10390

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
Third Semester
Electrical and Electronics Engineering
EE 8351 – DIGITAL LOGIC CIRCUITS
(Common to Electronics and Instrumentation Engineering/Instrumentation and Control Engineering)
(Regulations 2017)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2 = 20 Marks)**

1. A 16-bit data word given by 1001100001110110 is to be transmitted by using a fourfold repetition code. If the data word is broken into four blocks of four bits each, then write the transmitted bitstream.

2. Draw the circuit diagram of standard TTL NAND gate.

3. Write minterm and maxterm Boolean functions expressed by f(A, B, C) = Π(0, 3, 7).

4. Write the truth table of a full subtractor.

5. Compare level triggered flip flops and edge triggered flip flops.

6. Draw the timing diagram of four bit binary ripple counter each flip flop outputs.

7. When dynamic hazard occurs in digital circuits ?

8. Determine the size of the PROM required for implementing a dual 8 to 1 multiplexer with common selection inputs logic circuits.

9. Explain in words and write HDL statements for the operations specified by the following register transfer notation : If ($S_1 = 1$) then ($R_0 \leftarrow R_1$) else if ($S_2 = 1$) then ($R_0 \leftarrow R_2$).

10. What is the use of repeat statement in Verilog HDL ?

PART – B **(5×13 = 65 Marks)**

11. a) i) Find the decimal equivalent of the following binary numbers expressed in the 2's complement format, 00001110; 10001110. **(3)**

ii) Explain in detail about cyclic redundancy check code for digital code transmission and reception. **(5)**

iii) Explain in detail about Ex-NOR gate and draw the CMOS logic diagram of it. **(5)**

(OR)

b) i) Why is ECL called nonsaturating logic ? What is the main advantage accruing from this ? With the help of a relevant circuit schematic, briefly describe the operation of ECL OR/NOR logic. **(6)**

ii) With neat internal schematic diagram explain BiCMOS logic two input NAND gate. **(7)**

12. a) i) Apply suitable Boolean laws and theorems to modify the expression for a two-input EX-OR gate in such a way as to implement a two-input EX-OR gate by using the minimum number of two-input NAND gates only. **(6)**

ii) Write a simplified maxterm Boolean expression for $\Pi(0, 4, 5, 6, 7, 10, 14)$ using the Karnaugh mapping method. **(7)**

(OR)

b) i) Find the minterms of the following Boolean expression by first plotting the function in a map : $F = C'D + ABC' + ABD' + A'B'D$. **(5)**

ii) Design a 4 bit gray to binary code converter. **(8)**

13. a) i) Explain in detail about master slave D flip flop with neat diagram. **(5)**

ii) A four-bit ring counter and a four-bit Johnson counter are in turn clocked by a 10 MHz clock signal. Determine the frequency and duty cycle of the output flip-flop in the two cases. **(8)**

(OR)

b) i) With the help of a schematic arrangement, explain how a J-K flip-flop can be used as a T flip-flop. **(6)**

ii) Three four-bit BCD decade counters are connected in cascade. The MSB output of the first counter is fed to the clock input of the second counter, and the MSB output of the second counter is fed to the clock input of the third counter. If the counters are negatively edge triggered and the input clock frequency is 256 kHz, what is the frequency of the waveform available at the MSB of the third counter ? **(7)**

14. a) i) Design a binary ripple counter that counts 000 and 111 and skips the remaining six states, that is 001, 010, 011, 100, 101 and 110. Use presentable, clearable negative edge-triggered J-K flip-flops with active LOW PRESET and CLEAR inputs. Also, draw the timing waveforms and determine the frequency of different flip-flop outputs for a given clock frequency, f_c. **(8)**

ii) You have two two-bit binary numbers A_1A_0 and B_1B_0. Design a PLA device to implement a magnitude comparator to produce outputs for A_1A_0 being 'equal to', 'not equal to', 'less than' and 'greater than' B_1B_0. **(5)**

(OR)

b) i) What are complex programmable logic devices (CPLDs) ? Briefly outline salient features of these devices and application areas where these devices fit the best. **(7)**

ii) Show that a BCD ripple counter can be constructed using a four-bit binary ripple counter with asynchronous clear and a NAND gate that detects the occurrence of count 1010. **(6)**

15. a) i) What is a hardware description language ? What are the requirements of a good HDL ? Briefly describe the salient features of VHDL and Verilog. **(8)**

ii) Write the VHDL code for four bit adder circuit. **(5)**

(OR)

b) i) Explain in detail about ASMD chart for digital system design. **(5)**

ii) Explain in detail about ASM block with an example. **(8)**

PART – C **(1×15 = 15 Marks)**

16. a) i) Design a synchronous counter that counts as 000, 010, 101, 110, 000, 010, ... Ensure that the unused states of 001, 011, 100 and 111 go to 000 on the next clock pulse. Use J-K flip-flops. What will the counter hardware look like if the unused states are to be considered as 'don't care's ? **(10)**

ii) Implement a full adder circuit using a 3-to-8 line decoder. **(5)**

(OR)

b) i) What is a clocked J-K flip-flop ? What improvement does it have over a clocked R-S flip-flop ? **(5)**

ii) Implement the three-variable Boolean function $F(A,B,C) = \overline{A}.C + A.\overline{B}.C + A.B.\overline{C}$ using a 4-to-1 multiplexer. **(5)**

iii) It is required to transmit letter 'A' expressed in the seven-bit ASCII code with the help of the Hamming (11, 7) code. Given that the seven-bit ASCII notation for 'A' is 1000001 and that the data word gets corrupted to 1010001 in the transmission channel, show how the Hamming code can be used to identify the error. Use even parity. **(5)**

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