UNIT I NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES

PART-A

1. How many bits are required to represent the decimal numbers in the range 0 to 999 using Straight binary codes and using BCD codes? How is the letter A coded in the ASCII code?

$(999)_{10}$= (1111100111 $)_2$→ 10 bits are required to represent decimal number in the range 0 to 999 using straight binary code

$(999)_{10}$= (1001 1001 1001)$_{BCD}$→ 12 bits are required to represent decimal number in the range 0 to 999 using BCD code

7-bit ASCII code for the Letter A is 1000001

2. Show that the excess-3code is self-complementing.

Self-complementing property: 1's complement of Excess-3 code of a decimal digit is equal to Excess -3 code of 9's complement of the corresponding decimal digit.

Example:

a. Excess -3 code of the decimal digit 2 = 0101

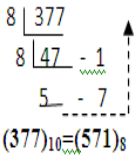
b. 1's complement of 0101 = 1010 ----------(1)

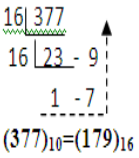
c. 9's complement of 2 = 9-2 = 7

d. Excess -3 code of 7 = 1010 ----------(2)

e. The self-complementing property of Excess -3 code is proved from equations (1)&(2).

3. Determine $(377)_{10}$ in Octal and Hexa-decimal equivalent.(Nov 2014)





4. Add the decimals 67 and 78 using excess-3 code.

67 = (0110 0111)$_{BCD}$= (1001 1010)$_{XS-3}$

78 = (0111 1000)$_{BCD}$= (1010 1011)$_{XS-3}$

---

1 0100 0101(+)

0011 0011 0011

(0100 0111 1000)$_{XS-3}$

5. Add the decimals 57 and 68 using 8421BCD code.

$57 = (0101\ \ 0111)_{BCD}$

$68 = (0110\ \ 1000)_{BCD}$

1011 1111(+)

0110 0110

$(0001\ \ 0010\ \ 0101)_{BCD}$

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6. What is meant by weighted and non-weighted code?

Weighted codes are those, which obey the positional weighting principles. In weighed code, each position of the number represents a specific weight. Example: 8421 & 2421

Non-Weighted Codes are codes that are not positionally weighted. Each position of the number is not assigned a fixed value.

Example: Excess-3 & Gray code

7. What is Gray code &mention the advantages and application of Gray code (Nov 2017)

The gray code is non-weighted code, which means that there are no specific weights assigned to the bit positions. In gray code, only one bit changes from one number to the next.

Advantages of Grey Code:

Switching activity is reduced because of one digit change in consequence code words. Low power consumption, Fast response & Minimum error in coding are the advantages of grey code.

Application:

Shaft position encoder in which analog data are represented by continuous change of a shaft position. The shaft is partitioned into segments, and each segment is assigned a number.

8. Convert the following hexadecimal numbers into decimal numbers: 263 and 1C3 (May2012)

$263_H = 2x16^2+6x16^1+3\ x16^0 = (611)_{\mathbf{10}}$

$1C3_H = 1x16^2+12x16^1+3x16^0 = (451)_{\mathbf{10}}$

9. Which gates are called as the universal gates? What are its advantages?

The NAND and NOR gates are called as the universal gates. These gates are used to perform any type of logic operations like AND, OR,NOT, etc.

10. Give the classification of logic families.

The classifications of logic families are

(i) Saturated Logic Family (ii)Non Saturated Logic Family

S.No	**Saturated Logic Family**	**Non-Saturated Logic Family**
1)	Register Transistor Logic(RTL)	1)Schottky TTL
2)	Diode Transistor Logic (DTL)	2)Emitter Coupled Logic(ECL)
3)	Transistor Transistor Logic (TTL)	

11. i)Convert $(11001010)_2$ into gray code. ii) (11101101) gray code into binary code.

Binary to Gray code conversion: $(11001010)_2 = (10101111)_{\text{Gray Code}}$

Gray to Binary code conversion: $(11101101)_{\text{Gray Code}} = (10110110)_2$

12. Mention the important characteristics of digital IC's?

The important characteristics of digital IC's are Fan out, Power dissipation, Propagation Delay, Noise Margin, Fan In, Operating temperature and Power supply requirements.

13. Define Fan- In and Fan-Out?(Nov 2015)(May 2016)

Fan- In is the number of inputs connected to the gate without any degradation in the voltage level. Fan- Out is defined as the maximum number of inputs of several gates that can be driven by the output of logic gate maintaining its output levels within the specified limits.

14. Define power dissipation and noise margin?

Power dissipation is measure of power consumed by the gate when fully driven by all its inputs. It is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output. It is expressed in volts.

15. What is propagation delay?(Apr 2015)

Propagation delay is the average transition delay time for the signal to propagate from input to output then the signals change in value. It is expressed in ns.

16. Mention the characteristics of MOS transistor?

The n- channel MOS conducts when its gate- to- source voltage is positive. The p-channel MOS conducts when its gate- to- source voltage is negative. Either type of

device is turned off if its gate- to- source voltage is zero.

17. Why totem pole outputs cannot be connected together?

Totem pole outputs cannot be connected together because such a connection might produce excessive current and may result in damage to the devices.

18. State advantages and disadvantages of TTL

Advantages: Easily compatible with other ICs, Low output impedance.

Disadvantages: Wired output capability is possible only with tri state and open collector type special circuits in Circuit layout and system design are required.

19. What is the advantages of ECL over TTL?(Nov 2014)

Transistors in ECL logic families do not saturate which eliminates the storage time delay. So ECL families have the fastest operating speed and the propagation delay time per gate is approximately 1nsec while that of TTL is 12 nsec.

20. Compare the totem pole output with open collector output. (Nov 2014)

Totem pole	**Open collector**
Output stage consists of Pull up transistor, Diode resistor and pull - down transistor.	Output stage consists of only pull down transistor.
External pull-up resistor is not required.	External pull-up resistor is required
Output of two gates cannot be tied together.	Output of two gates can be tied together using wired AND technique.
Operating speed is high.	Operating speed is low.

21. Convert: a) $(475.25)_8$ to its decimal equivalent & b) $(549.B4)_{16}$ to its binary equivalent (Apr 2015)

(a) $(475.25)_8$ to its decimal equivalent

$(475.25)_8 = 4x8^2+7x8^1+5x8^0+2x8^{-1}+5x8^{-2}$

$=256+56+5+0.25+0.078125$

$=(317.32814)_{10}$

(b) $(549.B4)_{16}$ to its binary equivalent

$(549.B4)_{16}=5x16^2+4x16^1+9x16^0+11x16^{-1}+4x16^{-2}$

$=261+64+9+0.6875+0.01562$

$= (334.703)_{10}$

2|334

2 167 --- 0
2 83 ---1
2 41 ---1
2 20 ---1
2 10 ---0
2 5 ----0
2 2 ----1
1 ----0

0.703*2 =1.406 ------1

0.406*2=0.81 ---------0

0.81*2=1.62 ----------1

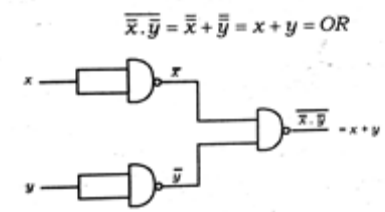
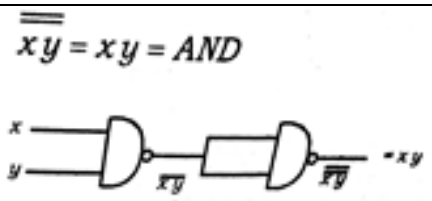
0.62*2=1.24----------1

0.24*2=0.48----------0

0.48*2=0.96----------0

Binary equivalent of 334.703 = 101001110 .101100

22.Construct OR gate and AND gate using NAND gate. (Nov 2016)

OR Gate	AND Gate
	

23.What is unit distance code? Give an example. (Nov 2015)

Unit distance code is a non- weighted code in which next increment or decrement causes the bit transition only at one place. Ex: Gray code.

24.Convert the following binary code into gray code 1010111000_2. (May 2016)

⊕ ⊕ ⊕ ⊕ ⊕ ⊕ ⊕ ⊕ ⊕

Binary : 1 → 0 → 1 → 0 → 1 → 1 → 1 → 0 → 0 → 0

↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓

Gray: 1 1 1 1 1 0 0 1 0 0

25. Convert $(115)_{10}$ and $(235)_{10}$ to hexadecimal numbers. (Nov 2017)

16 | 115

7 ------ 3

$(115)_{10} = (73)_{16}$

16 | 235

14(E) ------11(B)

$(235)_{10}$ **$=(EB)_{16}$**

25.Convert the following Excess 3 numbers into decimal numbers. (Nov 2016)

a) 1011

- 0011

$1000 = (8)_{10}$

b) 1001 0011 0111

- 0011 0011 0011

$0100\ 0000\ 0100 = (404)_{10}$

26. Reduce a (b+bc') + ab'. (Apr 2017)

a (b+bc') + ab' = ab(1+c')+ ab'

= ab+ab'

= a (b+b') = a

27. Convert 143_{10} into its binary and binary coded decimal equivalent. (Apr 2017)

2 | 143

2 | 71 ----------1

2 | 35 ---------- 1

2 | 17 --------- 1

2 | 8 ---------1

2 | 4 -------- 0

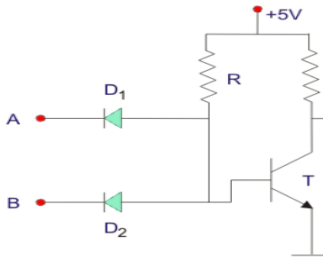
2 | 2----------0

1----------0

$(143)10 = (10001111)_2$

The binary coded Decimal of $(143)_{10}$ is 0001 0100 0011

28. Draw the DTL based NAND gate. (Nov 2018)



29. Perform subtraction on the following unsigned binary numbers using 2's

complement of subtrahend (a) 11011- 11001 (b) 110100- 10101. (Nov 2019)

a) 11011- 11001

1's complement of 11001 =00110

2's Complement of 11001 =(1's complement of 11001+1) =00111

Add 00111 with 11011

1 1 1 1

1 1 0 1 1

0 0 1 1 1 (+)

---

1 0 0 0 1 0

Eliminate the carry

Ans =11011-11001 =00010

b)110100- 10101

1's complement of 010101 =101010

2's Complement of 11001=01010+1=101011

Add 101011 with 110100

1 1 0 1 0 0 (+)

1 0 1 0 1 1

---

1 0 1 1 1 1 1

Eliminate Carry

Ans = 011111

30. List the different types of output configuration in TTL (Nov 2019)

There are three different types of output configuration in TTL. They are

(i) Totem pole configuration

(ii) Open Collector configuration

(iii) Tristate configuration

31. Convert $(101.01)_2$ to decimal number. (April 2019)

$(101.01)_2 = [(1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0) + (0 \times 2^{-1}) + (1 \times 2^{-2})]_{10} = 5.25_{10}$.

32. Give each one example for error detecting code and error correcting code. (April 2019)

Error detection codes

Error Correction codes are used to detect the errors present in the received data bit

stream. These codes contains some parity bits which are appended to the original data bit stream. These codes detect the error, if it is occurred during transmission of the original data bitstream .Examples : Parity code, Hamming code.

Error correction codes-

Error correction Codes are used to correct the errors present in the received data bitstream. Error correction codes also use the similar strategy of error detection codes. Example − Hamming code.

33. A 16-bit data word given by 1001100001110110 is to be transmitted by using a four fold repetition code. if the data word is broken into four blocks of four bits each, then write the transmitted bitstream. (Nov 2020)

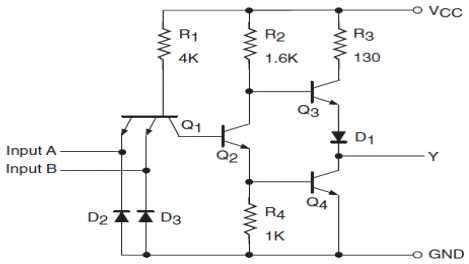
Given 16 bit data : 1001100001110110

Data word is broken into four blocks of four bits each : 1001 1000 0111 0110

Four fold repetition code :

10011001 1001 1001 1000 1000 1000 1000 0111 0111 0111 0111 0110 0110 0110 0110

34. Draw the circuit diagram of standard TTL NAND gate.(Nov 2020)



PART-B (C201.1)

1. Explain the characteristics and implementation of the given digital logic families: (i) DTL and (ii) RTL **(Apr 2018)**

2. Explain the basic working principles of following digital logic families. (i) TTL (ii) ECL and (iii) CMOS **(May 2013) (Nov 2019)**

3.(i) State the differences between 1's complement and 2's complement subtraction with suitable examples.

(ii) Explain about error detection and correction codes. **(Nov 2017)**

4. (i) Given that a frame with bit sequence 1101011011 is transmitted, it has been received as 1101011010. Detect the error using any one error detecting code.

(ii) Draw the MOS logic circuit for NOT gate and explain its operation**.(Nov 2014)**

5. (i) Explain the Hamming code with an example. State its advantages over parity codes.

(ii) Design a TTL logic circuit for a 3 input and 2 input NAND gate. **(Nov 2014) (Apr 2017)**

6. Explain the two types of MOS families. **(Nov 2019)**

7. (i) A 12 bit hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8 bit data word that was written into memory if the 12 bit word read out is as (1) 101110010100 and (2) 111111110100.

(ii) Briefly discuss weighted binary code. **(Nov 2015)**

8. (i) Perform the following addition using BCD and Excess-3 addition (205+569).

(ii) Encode the following binary word 1011 into seven bit even parity hamming code**. (Apr 2015)**

9. (i) With circuit schematic ,explain the operation of a two input TTL NAND gate with totem pole output. **(Nov 2018)**

(ii)Compare totem pole and open collector outputs. **(Apr 2015) (Apr 2017)**

10. (i) Explain with an aid of circuit diagram the operation of 2 input CMOS NAND gate and list out its advantages over other logic families.

(ii) Given the two binary numbers X=1010100 and Y=1000011, perform the subtraction Y-X using 2's complements. **(Nov 2016)**

11. (i) Explain in detail the usage of hamming codes for error detection and error correction with an example considering the data bits as 0101.

(ii) Convert $FACE_{16}$ into its binary octal and decimal equivalent. **(Apr 2017)**

12. With circuit schematic and explain the operation and characteristics of an ECL. **(May 2016)**

13. (i) Convert 1010111011101100_2 into its octal, decimal and hexadecimal equivalent.

(ii) Deduce the odd parity hamming code for the data: 1010. Introduce an error in the LSB of the hamming code and deduce the steps to detect the error. **(May 2016)**

14. Give different arithmetic operator and bitwise operator**. (Apr2018)**

15. Assume a 3 input AND gate with output F and a 3 input OR gate with G output. Show the signals of the output F and G as functions of the 3 inputs ABC. Use all 8 possible combinations of the inputs ABC. **(Nov 2018)**

16. Show that a possible logic NAND gate is a negative logic NOR gate and vice versa. **(Nov 2018).**

17. Design a CMOS inverter and explain its operation. Comment on its characteristics such as Fan-in, Fan-out, power dissipation, propagation delay and noise margin. Compare its advantages over other logic families. **(Apr 2017)**

18. (i) Design a 3- input NAND gate circuit using TTL Logic.

(ii) Explain in detail the generation of hamming code for 4- bit data. **(April 2019)**

19. (i) Design a 2-input NOR gate using CMOS logic. (ii) Explain the operation of RTL inverter circuit with relevant diagrams. **(April 2019)**

20.i) Find the decimal equivalent of the following binary numbers expressed in the 2's complement format, 00001110; 10001110.(3)

ii)Explain in detail about cyclic redundancy check code for digital code transmission and reception.(5)

iii)Explain in detail about Ex-NoR gate and draw the cmoS logic diagram of it.(5) (Nov 2020)

21. i) Why is ECL called non-saturating logic ? What is the main advantage accruing from this ? With the help of a relevant circuit schematic, briefly describe the operation of ECL OR/NOR logic.(6)

ii) With neat internal schematic diagram explain BiCMOS logic two input NAND gate.(7)

22. It is required to transmit letter 'a' expressed in the seven-bit ASCII code with the help of the Hamming (11, 7) code. given that the seven-bit ASCII notation for 'a' is 1000001 and that the data word gets corrupted to 1010001 in the transmission channel, show how the Hamming code can be used to identify the error. Use even parity.(5) (Nov 2020)

UNIT II COMBINATIONAL CIRCUITS

PART-A

1. Simplify the expression: X = (A'+B)(A+B+D)D'.

X = (A'+B) (A+B+D) D' = (AA' + A'B + A'D + AB + BB + BD) D'

X = (0 + A'B + A'D + AB + B + BD) D'

X = (A'D + B (A' + A + 1 + D)) D' = (A'D + B) D'

X = A'DD' + BD' = 0 + BD' therefore X = BD'

2. Simplify Y = (A+B)(A'+C)

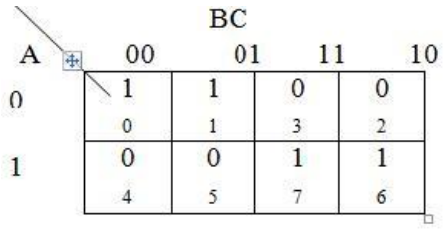
Y = (A+B) (A'+C) = AA' + AC + A'B + BC = 0 + AC + A'B + BC

Y = AC + A'B + BC = AC + A'B (using consensus theorem XY+X'Z+YZ=XY+X'Z)

3. What is a prime implicant?

A prime implicant is a product term obtained by combining the maximum possible number of adjacent squares in the map.

Example: The possible prime implicants in the following K-Map are A'B' & AB



4. Define the following: minterm and maxterm?

Minterm (standard product) is a combination of n variables using AND operation for the function of n variables. Possible minterms for a function of two variables A & B: A'B', A'B, AB', AB

Maxterm (standard sum) is a combination of n variables using OR operation for the function of n variables. Possible maxterms for a function of two variables A & B: A+B, A+B', A'+B, A'+B'

5. Simplify A+AB+A'+B.

A+AB+A'+B = A+A' + AB + B

= 1+ AB + B (X+X'=1)

= 1 (X+1 = 1)

6. Express x + yz as the sum of minterms.

x + yz = x (1) + (1)yz = x(y + y') + (x + x')yz = xy + xy' + xyz + x'yz

= xy(1) + xy'(1) + xyz + x'yz = xy(z + z') + xy'(z + z') + xyz + x'yz

= <u>xyz</u> + xyz' + xy'z + xy'z' + xyz + x'yz

=xyz + xyz' + xy'z + xy'z' + x'yz ----------(x + x = x)

=111 + 110 + 101 + 100 + 011 =m7 + m6 + m5 + m4 + m3

x + yz =∑m (3, 4, 5, 6, 7)

7. Describe the canonical forms of the Boolean function.

Sum of minterms: Combination of minterms using OR operation.

Example: F = A'B + AB = m_1 + m_3, F = ∑m (1, 3)

Product of maxterms: Combination of maxterms using AND operation.

Example: F = (A+B) (A'+B) = M_0 M_2, F = ∏M (0, 2)

8. Give some of the major applications of multiplexers and decoders.(Nov 2014)

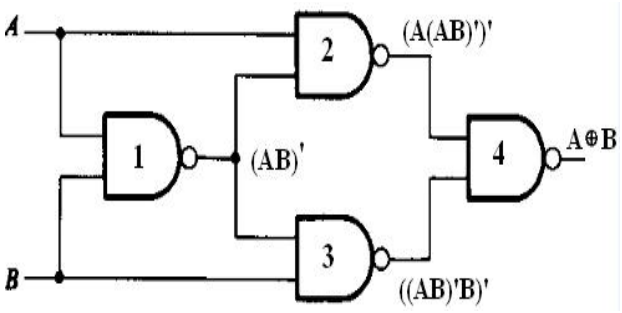
Multiplexers: Data selection, Data routing, parallel to serial conversion, Logic-function generation. **Decoders:** Memory addressing, Instruction decoding.

9. Express f(a,b,c) = a+b'c as sum of minterms

A	B	C	B'	B'C	A+B'C
0	0	0	1	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	1	0	0	1

f (a,b,c) = ∑m(1, 4, 5, 6, 7)

10. Draw the logical diagram for Ex- OR gate using NAND gates.(Nov 2015)



11. Simplify the expression Z=AB+AB'(A'C')'(Apr 2015)

Z=A (B+B' (A'C')')

=AB+ AB' (A+C) (Demorgan's Law)

= A (B+ B' (A+C)) [A+ A'B=A+B] Z= A(B+ A+C)

= A+A (B+C) [A+ AB=A] Z=A

12. Convert the given expression in canonical SOP from Y= AB+A`C+BC`. (Nov 2015)(Nov 2016)

Y = AB+A`C+BC`

=AB (C + C') + A`C (B + B') + BC` (A + A')

=ABC+AB C'+ A`BC+ A` B'C+ A BC` + A' BC`

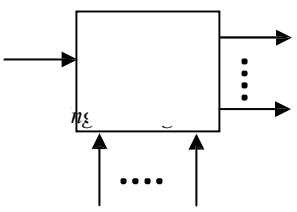
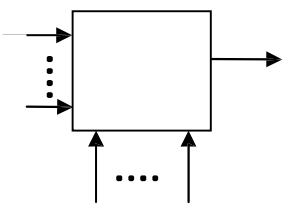
= ABC+ABC`+A`BC+A`B`C+A`BC`. [A + A =A] = ∑(1,2,3,6,7)

13.Reduce A · (A + B). (Apr 2018)

A · (A + B) = AA+AB

= A+AB = A (1+ B) = A.

14. Mention the difference between a DEMUX and a MUX.

DEMUX	MUX
	

Block diagram: Single Input 1×2^n n selection inputs 2^n Outputs	2^n Inputs $2^n \times 1$ Single output n selection inputs
A demultiplexer is a circuit that receives information on a single line and transmits this information on one of many output lines	A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line.
Data Distributor	Data selector

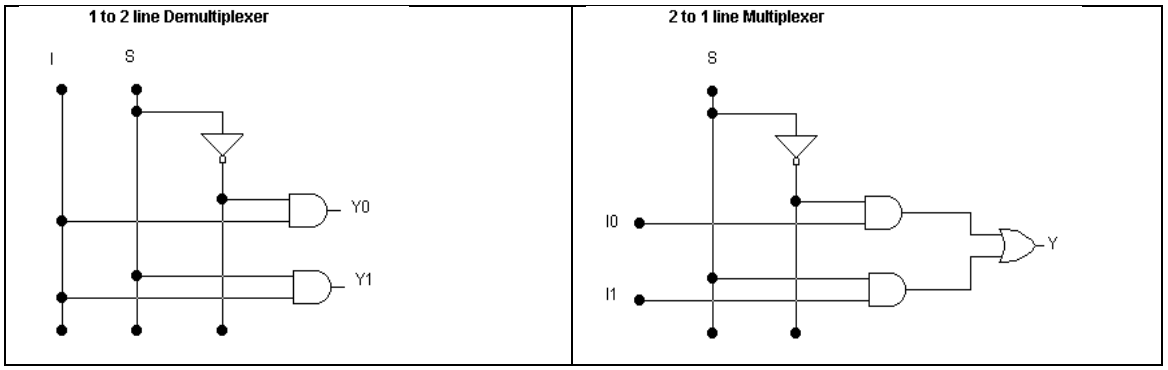
15. What is K map? (Apr 2018)

A Karnaugh Map (K-Map) is a pictorial method used to minimize Boolean expressions without having to use Boolean algebra theorems and equation manipulations.

16. Draw the truth table of 2: 1 MUX. (Nov 2016)

Input		**Output**
e	**S**	**Y**
1	**0**	**D_0**
1	**1**	**D_1**
0	**X**	**0**

17. Draw a 1 to 2 demultiplexer circuit and 2 to 1 multiplexer circuit.

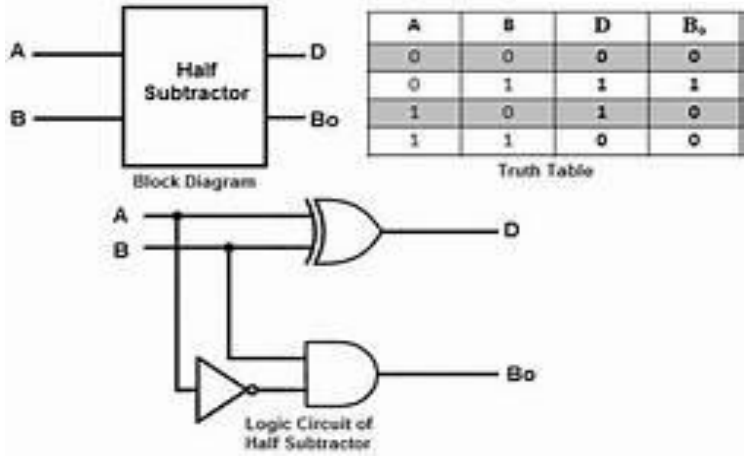


18. State the Associative property of boolean algebra. (Apr 2018)

$A + (B + C) = (A + B) + C$

$A \cdot (B \cdot C) = (A \cdot B) \cdot C$

19. Design a half subtractor. (May 2016) (Apr 2017)



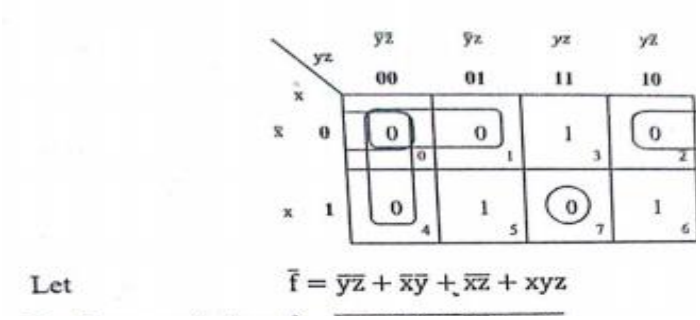
A	B	D	B_o
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Truth Table

20. Compare Decoder and DEMUX (Nov 2017)

DECODER	DEMUX
A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines.	A demultiplexer is a circuit that receives information on a single line and transmits this information on one of many output lines
A decoder accepts a set of binary inputs and activates only the output that corresponds to that input number. Example: Binary to Octal decoder	Demux is used as a Data Distributor. Example: Serial to parallel converter.

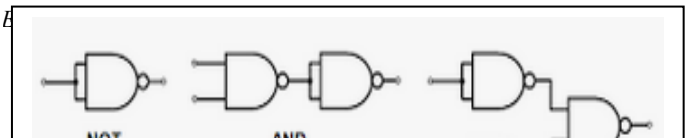
21. Write the POS form of the SOP Expression f(x,y,z) = x'yz+xyz'+xy'z. (Apr 2017)



22. Define Duality Property (Apr 2018)

The principle of duality in Boolean algebra states that if you have a true Boolean statement (equation) then the dual of this statement (equation) is true. The dual of a boolean statement is found by replacing the statement's symbols with their counterparts. This means a "0" becomes a "1", "1" becomes a "0", "+" becomes a "." and "." becomes a "+".

23. Draw the NAND gate circuit using NOT, AND & OR Gates. (Nov 2018)



24.Mention the dependency of output in combinational circuits. (Nov 2018)

In combinational circuits, the output depends only on the present value of input. But in case of sequential circuits output depends on present input and past output.

25. Determine the exact number of half adders and full adders required for performing the addition of two binary number of 5-bit length each. (April 2019)

Addition of two binary number of 5-bit length each need

(i) Number of Full adder = 4 and

(ii) Number of Half adder = 1.

26. Find the result of A+A'D+AC'. (April 2019)

A+A'D+AC'= A(1+C')+ A'D

=A+A'D

=A+D

27. Write minterm and maxterm Boolean functions expressed by f(a, B, c) = Π(0, 3, 7).(Nov 2020)

Maxterm

	B'C'	B'C	BC	BC'
A'	0	1	0	1
A	1	1	0	1

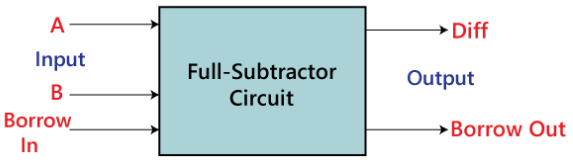
Maxterm = (BC+A'B'C')'

=(B'+C') (A+B+C)

Minterm = B'C'+BC'+AC'

28. Write the truth table of a full subtractor (Nov2020)

Inputs			Outputs	
A	B	$Borrow_{in}$	Diff	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



PART B (C201.2)

1. (i) Design 4 bit Gray Code to binary converters using logic gates.

(ii) Excess-3 Code converter using NAND gates. **(Nov 2017)**

2. a. Design BCD to Excess-3 code converter**. (Apr 2015)(Nov 2015)**

3. What are Magnitude comparators? Explain the design of magnitude comparators with the help of a suitable example. Construct 16-bit comparator using 4-bit comparator as a building block.

4. (i)Prove that ABC+ABC'+AB'C+A'BC =AB+AC+BC.

(ii)Convert the given expression on canonical SOP form Y= AC+AB+BC. **(Apr 2018)**

5. Design a full subtractor and implement using logic gates. Also implement the same using half subtractors. **(Nov 2014) (Nov 2015) (Nov 2016)**

6. (i) Show that a function expressed as a sum of its min terms is equivalent to a function expressed as a product of its max terms.

(ii)Using K-map simplify the following function and implement the function using logic gates f (A, B, C) = ∏(0, 4, 6).**(Nov 2012)**

7. Prove that for constructing XOR from NANDs we need four NAND gates. **(May 2013)**

8. (i)Implement the function F(p,q,r,s)=Σ(0,1,2,4,7,10,11,12) using decoder.**(Nov 2014)**

(ii)Design a 4 bit Binary to gray code converter and implement using logic gates.

9. Simplify the Boolean function using K-map and implement using only NAND gates. F(A,B,C,D)= Σm(0,8,11,12,15)+ Σd(1,2,4,7,10,14) (Nov 2015). Mark the essential and non essential prime implicants.

10. Implement the Boolean function using 8:1 mux: F(A,B,C,D)=Σm(0,1,3,4,8,9,15) **(Apr 2015)**

11. Simplify the logical expression using K map in SOP and POS form

F(A,B,C,D) = Σm(0,2,3,6,7)+ d(8,10,11,15). **(Nov 2016).**

12. (i) simply the following function using karnaugh Map.

f(w,x,y,z) = Σm(0,1,3,9,10,12,13,14)+ Σd(2,5,6,11).

(ii) Implement the following function using only NAND gates: f(x,y,z) = Σm(0,2,4,6). **(May 2016)**

13. (i) Design a BCD to EXCESS 3 code converter.

(ii) Design a full adder and implement it using suitable multiplexer.**(Nov 2017)**

14. Design a half subtractor circuit with inputs x and y and outputs D and B.The circuit subtracts the bits x-y and places the difference in D and the borrow in B **(Nov 2019)**

15. (i)Reduce the following function using K-map. f(A,B,C,D)= ∏M(0,2,3,8

,9,12,13,15)

(ii)Design a full adder using two half adders and an OR gate. **(Apr 2015)**

16. Simplify the following Expressions in 1)Sum of products 2)Product of Sums

a) x'z'+y'z'+yz'+xy

b) AC'+B'D+A'CD+ABCD

c) (A'+B'+D')(A+B'+C')(A'+B+D')(B+C'+D') **(Nov 2019)**

17. Simplify the Boolean function using K-map F(w,x,y,z))=Σ (0,1,3,5,6,7,8,12,14) which has the don't care conditions d(w,x,y,z)= Σ(9,15). **(Apr 2017)**

(ii) Design the Boolean function f(a,b,c)= Σ (3,7,4,5) and implement it using suitable multiplexer. (**Apr 2017)**

18. i) Design a 3*8 decoder and explain its operation as a minterm generator.

ii) Design a full adder using NOR gates. **(Apr 2017)**

19. Write down the steps in implementing a Boolean function with levels of AND gate. **(Apr 2018)**

20. Give the general procedure for converting a Boolean expression into multilevel NAND diagram. **(Apr 2018)**

21. Given the following Boolean functions F=A'C+A'B+AB'C+BC.

i) Express it in sum of Min terms.

ii) Find the minimal sum of products expression. **(Nov 2018)**

22. Draw the logic diagram of 2 to 4 line Decoder using NOR gates only. Include an enable input. **(Nov 2018)**

23. Design a combinational circuit with three inputs x,y and z and three outputs A,B and C. When the binary input is 0,1,2 or 3 the binary output is one greater than the input. When the binary input is 4,5,6 or 7 the binary output is one less than the input. **(Nov 2018)**

24. (i) Design a 3×8 decoder using 2×4 decoders. Draw the truth table.

(ii) Design a full adder circuit using logic gates. **(Apr 2019)**

25. (i) Simplify and implement the logic function F(A, B, C)= ∑(0, 1, 4, 5, 7) using logic gates.

(ii) Design a 4×2 priority encoder using logic gates. **(Apr 2019)**

26. i) Apply suitable Boolean laws and theorems to modify the expression for a two-input Ex-OR gate in such a way as to implement a two-input Ex-OR gate by using the minimum number of two-input NAND gates only.(6)

ii) Write a simplified maxterm Boolean expression for Π(0, 4, 5, 6, 7, 10, 14) using the Karnaugh mapping method. (Nov 2020)

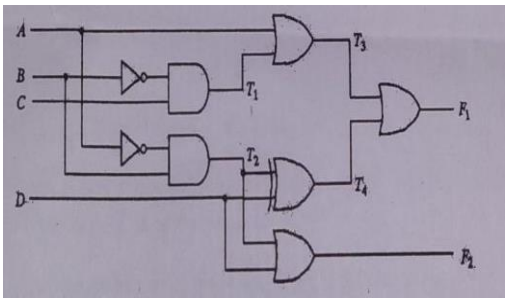
27. Design a 4 bit gray to binary code converter. (Nov 2020)

28. Simplify the following function and implement it using NAND gates only; F(w, x, y, z)= ∑(1, 3, 5, 7, 9, 11,13,15), with don't care states d(w, x, y,z)= ∑(0, 2, 4, 6, 8). **(Apr 2019)**

29. Consider the combinational circuit shown in fig

i) Derive the Boolean Expression for T1 through T4. Evaluate the outputs of F1 and F2 as a function of the four inputs.

ii) List the truth table with 16 binary combinations of the four inputs variables .Then list the binary values fotT1 through T4 and outputs F1 and F2 in the table.Plot the output Boolean function obtained in part (b) on maps and show that the simplified Boolean expressions are equivalent to the ones obtained in part (a) **(Nov 2019)**



30. Implement a full adder circuit using a 3-to-8 line decoder. (5) **(Nov 2020)**

Implement the three-variable Boolean function using 4:1 MUX

F(A,B,C) =A'C+AB'C+ABC' (5) (Nov 2020)

UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS

PART A

1. What is the classification of sequential circuits?

The sequential circuits are classified on the basis of timing of their signals into two types. They are, 1) Synchronous sequential circuit. 2) Asynchronous sequential circuit.

2. Define Flip flop. What are the different types of flip-flop?

The basic unit for storage is flip flop. A flip-flop maintains its output state either at 1 or 0 until directed by an input signal to change its state.

Types:1. RS flip-flop 2. SR flip-flop 3. D flip-flop 4. JK flip-flop 5. T flip-flop

3. What is the operation of JK flip-flop? Why it is called a universal flip-flop. (Nov 2012)

- When K input is low and J input is high the Q output of flip-flop is set.

- When K input is high and J input is low the Q output of flip-flop is reset.
- When both the inputs K and J are low the output does not change.
- When both the inputs K and J are high it is possible to set or reset the flip-flop (ie) the output toggle on the next positive clock edge.The flip flop can be realized using any type of gates. NAND or OR

4. Define race around condition. (Nov 2017)

In JK flip-flop output is fed back to the input. Therefore change in the output results change in the input. Due to this in the positive half of the clock pulse if both J and K are high then output toggles continuously. This condition is called 'race around condition'.

5. What is edge-triggered flip-flop?

The problem of race around condition can solved by edge triggering flip flop. The term edge triggering means that the flip-flop changes state either at the positive edge or negative edge of the clock pulse and it is sensitive to its inputs only at this transition of the clock.

6. What is a master-slave flip-flop?(Apr 2018)

A master-slave flip-flop consists of two flip-flops where one circuit serves as a master and the other as a slave. The advantage for using a master-slave instead of a JK for toggling is the master-slave doesn't allow the output to change when q changes and waits for a clock pulse. This prevents false triggering that is referred to as "race".

7. Define rise time and fall time.

The time required to change the voltage level from 10% to 90% is known as rise time(t_r).The time required to change the voltage level from 90% to 10% is known as fall time(t_f).

8. Define skew and clock skew.

The phase shift between the rectangular clock waveforms is referred to as skew and the time delay between the two clock pulses is called clock skew.

9. Define sequential circuit?

In sequential circuits the output variables dependent not only on the present input variables but they also depend up on the past history of these input variables.

10. Define setup time.

The setup time is the minimum time required to maintain a constant voltage levels at the excitation inputs of the flip-flop device prior to the triggering edge of the clock

pulse in order for the levels to be reliably clocked into the flip flop. It is denoted as t_{setup}.

11. Define hold time.

The hold time is the minimum time for which the voltage levels at the excitation inputs must remain constant after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip flop. It is denoted as t_{hold}.

12. Why is gated D latch called transparent latch?

D	Q_{n+1}	Comments
0	0	Set
1	1	Reset

From the truth table of D flip flop it is found that, the output Q will look exactly like D. Hence, the D latch is said to be transparent latch.

13. What is the operation of D flip-flop and T flip-flop?

In D flip-flop during the occurrence of clock pulse if D=1, the output Q is set and if D=0, the output is reset.

T flip-flop is also known as Toggle flip-flop.

When T=0 there is no change in the output.

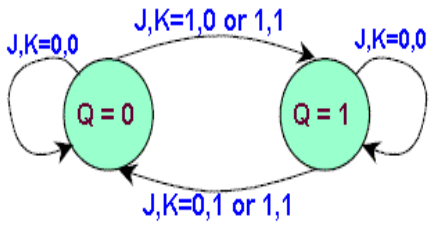
When T=1 the output switch to the complement state (ie) the output toggles.

14. Explain the flip-flop excitation tables for RS FF.

SR Flip-flop

Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

15. Draw the state diagram of JK flip flop? (Nov 2016)



16.Compare synchronous and asynchronous sequential circuit.

S.No	Synchronous Sequential circuits	Asynchronous Sequential circuits

1.	Clocked flip flops are used as memory elements	Either unclocked flip flops or time delay elements (latches) are used as memory elements.
2.	Change in input signals can affect memory element upon activation of clock signal	Change in input signals can affect memory element at any instant of time
3.	Clock frequency selection is based on total time delay. Hence slower response.	Because of absence of clock, faster Response
4.	Common clock pulse is given to all	No common clock pulse.

17. Give the comparison between combinational circuits and sequential circuits. (Nov 2019)

S. No.	**Combinational circuits**	**Sequential circuits**
1.	Output variables depend on the input alone.	The output variable depends on the present input and previous output
2.	Memory unit is not required	Memory unit is required to store the previous output.
3.	Faster response since propagation	Slower response due to the delay
4.	Simple design	Complex design
5.	Eg. Parallel adder	Eg. Serial adder

18.Compare level triggered flip flops and edge triggered flip flops.(Nov 2020)

Level triggering	**Edge triggering**
1. It is of two types -High level triggering -Low Level triggering 2. Flipflop circuits will change their outputs only when the clock is either at active high or low level.	1. It is of two types -Positive edge triggering -Negative edge triggering 2. Flipflop circuits will change their outputs only when there is either Positive edge or negative edge clock transition.

19. Draw truth table for D flip flop and JK flip flop. (May 2013)

J	**K**	**Q_{n+}**	**Comments**
0	0	Q_n	No Change
0	1	0	Reset
1	0	1	Set
1	1	Q'_n	Complement

D	**Q_{n+1}**	**Comments**
0	0	Set
1	1	Reset

20. Write the role Master clock generator in synchronous circuits. (Nov 2019)

Practical synchronous sequential logic systems use fixed amplitude such as voltage level for the binary signals. Synchronization is achieved by a timing device called a Master clock generator, which generate a periodic train of clock pulses.

21. Show how the JK flipflop can be modified into a D flip flop or a T flip flop. (Nov 2014)

From the truth table of JK flipflop, it is observed that when J=K, it operates similar to T flip flop and When J=K' it operates similar to D flip flop.

D	Q_{n+1}	Comments
0	0	Set
1	1	Reset

J	K	Q_{n+}	Comments
0	0	Q_n	No Change
0	1	0	Reset
1	0	1	Set
1	1	Q'n	Complement

T	Q_{n+}	Comments
0	Q_n	No Change
1	Q'n	Compleme

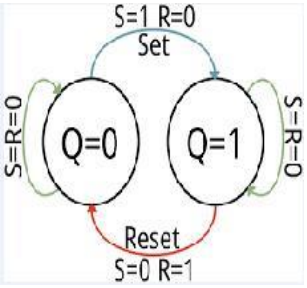
22. Differentiate between Mealy and Moore models. (May 2016)(Apr 2017).

Mealy models	Moore models
Output is a function of both the present	Output is a function of present state
In state diagram representation, both the input and output values are separated by a	Inputs alone are marked along the directed lines in their state diagram

23. Draw state diagram and give its characteristics equation and truth table of SR flip flop? (Nov 2015)(May 2016)

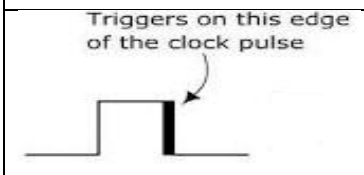
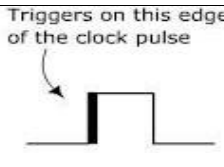
Truth table **State Diagram**

S	R	Next state of Q
X	X	No change
0	0	No change
0	1	Q = 0; reset state
1	0	Q = 1; set state
1	1	Indeterminate

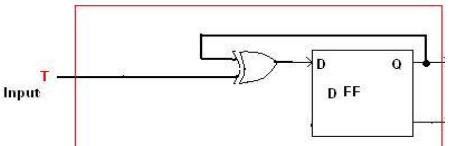


24. What is an edge triggered flip flop? (Nov 2015)

a. Edge triggered flip flop- Flip flops changes state either at positive edge (rising edge) or at negative edge (falling edge) of clock pulse and is sensitive to its inputs only at this transition of the clock.

Negative Edge	Positive Edge
	

25. Convert T Flip Flop to D Flip Flop. (Apr 2015)



26. What is a preset table counter and Ripple Counter (Nov 2017) (Nov 2018)

Preset Table Counter:

This counter can be cleared by a high level on the RESET line, and can be preset to any binary number present on the inputs by a high level on the PRESET ENABLE line.

Ripple Counter:

A **ripple counter** is an **asynchronous counter** where only the first flip-flop is clocked by an external clock. All subsequent flip-flops are clocked by the output of the preceding flip-flop. **Asynchronous** counters are also called **ripple**-counters because of the way the clock pulse **ripples** it way through the flip-flops.

27. Comparison between synchronous and asynchronous counter? (Apr 2018)

S.No	Synchronous Counter	Asynchronous Counter
1.	All flipflops are applied with same clock.	Different flipflops are applied with different clocks
2.	It is faster in operation	It is slower in operation
3.	Any count sequence is possible	Fixed count sequence either up or down.
4.	Produces no decoding error	Produces decoding error

28. Define synchronous sequential circuit (Nov 2019)

In sequential circuits the output variables dependent not only on the present input variables but they also depend up on the past history of these input variables. In synchronous sequential circuit ,change in input signals affect the memory element upon activation of clock signal. Clocked flip flops are used as memory elements. Common clock pulse is given to all the units in the design.

29. What is FSM? List its two basic types. (Apr 2019)

Finite State Machine's (FSMs) are at the heart of most digital design. The basic idea of an FSM is to store a sequence of different unique states and transition between them depending on the values of the inputs and the current state of the machine.

The FSM can be of two types:

(i) Moore FSM- where the output of the state machine is purely dependent on the state variables.

(ii) Mealy FSM- where the output can depend on the current state variable values and the input values.

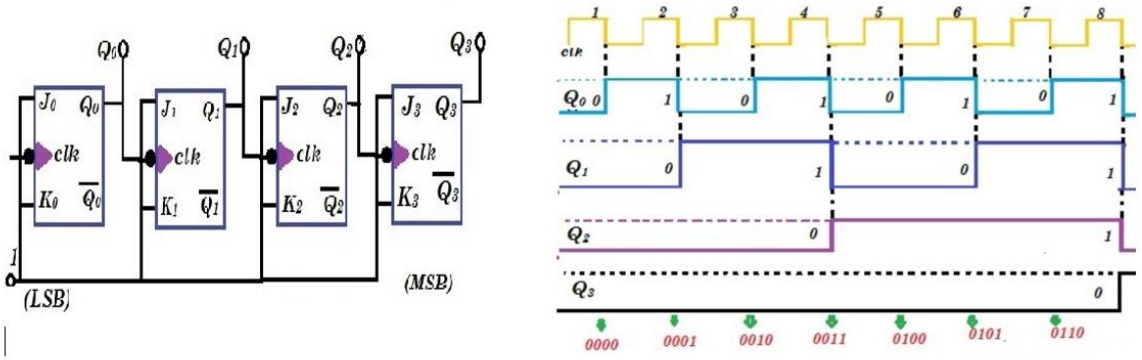
30.Write down the characteristics table of JK flip- flop. (Apr 2019)

The characteristics table shows the relationship between Flip- flop inputs, present state and next state. The characteristics table for JK Flip- Flop is given below:

Present State (Q_n)	**Next State (Q_{n+1})**	**Excitation Inputs**	
		J	**K**
0	0	0	0
0	0	0	1
0	1	1	0
0	1	1	1
1	1	0	0
1	0	0	1
1	1	1	0
1	0	1	1

31. Draw the timing diagram of four bit binary ripple counter each flip flop outputs.(Nov 2020)

Four bit ripple counter using JK flip flop



PART-B

1. (i)Explain T-flip-flop, SR Flip Flop and JK Flip Flop with suitable internal structure**.(Apr 2018)**

2. (i) Describe the difference between a gated S-R latch and an edge-triggered S-R flip flop.

(ii)Draw the logic circuits and the excitation tables for the T, JK flip-flops.

3. (i)Draw a master-slave J-K flip-flop system. Explain its operation and show that the race- around condition is eliminated **(Nov 2019) (Nov 2018)**

(ii)Draw the circuit of an S-R flip-flop using NAND gates. Modify it to include clock Derive

J-K circuit from S-R flip-flop circuit and explain its truth table.

4. (i)Explain what is universal shift register? Explain its working. (ii)Perform the following conversions T flip-flop to D flip-flop.

5. Explain in detail about shift Registers **(Nov 2017)(Apr 2017)**

6. (i)Design a BCD counter using JK flip-flops.

(ii)Design an up-down counter using D-flip-flops to count 0, 3, 2, 6, 4, and 0.

7. Design a 3-bit binary counter using T-flip flop **(May 2013).**

8. (i) Design an asynchronous Modulo-8 Down counter using JK flip flops**.(Nov 2014)**

(ii) Explain the circuit of SR flips flop and explain its operation.

9. (i) Design synchronous sequential circuit that goes through the count sequence 1,3,4,5 repeatedly. Use T flip flop for your design.

(ii) Explain the various types of triggering with suitable diagrams. Compare their merits and demerits. **(Nov 2014)(Nov 2017)**

10. Construct reduced state diagram for the following state diagrams. **(May 2013)**

11. (i)Design a synchronous decade counter using T flip flop and construct the timing diagram. (ii)Design a mealy model of sequence detector to detect the pattern 1001. **(Nov 2015)**

12. Draw and explain bit shift register. Also give it's truth table with it's input and output waveform. **(Apr 2018)**

13. (i)Design a MOD 5 Synchronous counter using JK flip flops.

(ii)Design a sequence detector to detect the sequence 101 using JK flip flop. **(Apr 2015)**

14. Design a sequence detector that produces an output '1' whenever the non overlapping sequence 101101 is detected**.(Nov 2016)**

15. Explain Flip Flop Excitation table for JK and RS Flip Flop **(Apr 2018)**

16. Design a MOD 5 Synchronous counter using T flip flops. **(May 2016)**

17. (i)Design a serial adder using mealy state model. (**May 2016)**

(ii)Explain the state minimization using portioning procedure with suitable example. **(May 2016)**

18. Assume that there is parking area in a sop whose capacity is 10. No more than 10 cars are allowed inside the parking area and the gate is closed as soon as the capacity is reached. There is a gate sensor to detect the entry of car which is to be synchronized with the clock pulse. Design and implement a suitable counter using JK flip flops. Also, determine the number of flip flops to be used if the capacity is increased to 50. **(Nov**

2016)

19. (i)A sequential circuit with two D flip flops A and B, input X and output Y is specified by by the following next state and output equations

A (t+1)= AX+BX, B(t+1)= A`X,

Y= (A+B) X`. Draw the logic diagram, derive state table and state diagram.

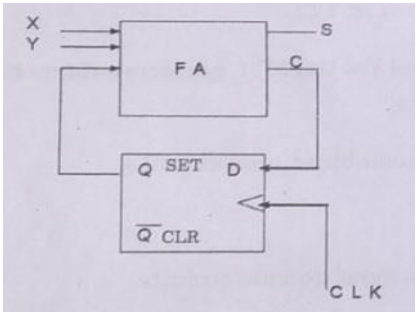
(ii) Realize T flip- flop using JK flip- flop. **(Nov 2015)**

20. Design a 5 bit Ring counter and mention its applications **(Apr 2017)**

21. Describe the design procedure with neat diagram about 4 bit bidirectional shift register with parallel load. **(Nov 2018)**

22. Design a sequential circuit with two D flip-flops A and B and one input X. When X=0, the state of the circuit remains same. When X=1, the circuit goes through the state transition from 00 to 01 to 11 to 10 back to 00 and repeats. **(Nov 2018)**

23. A sequential circuit has one flip flop Q ,two inputs x and y and one output S. It consists of a full adder circuit connected to a D Flip flop, as shown in figure. Derive the state table and state diagram of the sequential circuit. **(Nov 2019)**

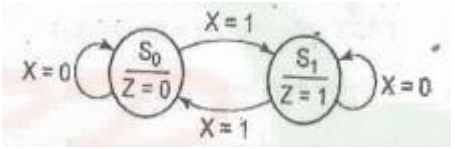


24. (i) Design a 2- bit synchronous sequential down counter.

(ii) Explain the operation of a 3- bit universal shift register. **(Apr 2019)**

25. (i) Explain Moore and Mealy models with the help of block diagrams.

(ii) Draw the state table for the following state diagrams. **(Apr 2019)**



26. Design a Modulo- 6 asynchronous binary up- counter. **(Apr 2019)**

27. i) With the help of a schematic arrangement, explain how a J-K flip-flop can be used as a T flip-flop.(6)

ii) Three four-bit BcD decade counters are connected in cascade. The MSB output of the first counter is fed to the clock input of the second counter, and the MSB output of the second counter is fed to the clock input of the third counter. if the

counters are **negatively** edge triggered and the input clock frequency is 256 kHz, what is the frequency of the waveform available at the mSB of the third counter ?(7) **(Nov 2020)**

28. i)Explain in detail about master slave D flip flop with neat diagram.(5)

ii) a four-bit ring counter and a four-bit Johnson counter are in turn clocked by a 10 MHz clock signal. Determine the frequency and duty cycle of the output flip-flop in the two cases. **(Nov 2020)**

29. Design a synchronous sequential logic circuit that goes through the sequence 0, 2, 4, 6, 8, 10, 12, 14 repeatedly. Use D flip- flop for your design. **(Apr 2019) .**

UNIT IV-ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABLE LOGIC DEVICES

PART A

1. Define secondary variables and excitation variables

The delay elements provide a short term memory for the sequential circuit. The present state and next state variables in asynchronous sequential circuits are called secondary variables. Excitation Variables are next state variables in asynchronous sequential circuits

2. What are races? (Nov 2012) or Define race conditions in asynchronous sequential circuit? (May 2013)(Nov 2016)

When 2 or more binary state variables change their value in response to a change in an input variable, race condition occurs in an asynchronous sequential circuit. In case of unequal delays, a race condition may cause the state variables to change in an unpredictable manner.

3. Define non critical and critical race.

If the final stable state that the circuit reaches does not depend on the order in which the state variable changes, the race condition is not harmful and it is called a non-critical race. If the final stable state depends on the order in which the state variable changes, the race condition is harmful and it is called a critical race.

4. What is a dead lock condition?(Nov 2014)

A condition resulting when one task is waiting to access a resource that another is holding, and vice versa. In an operating system, a deadlock occurs when a process or thread enters a waiting state because a requested system resource is held by another waiting process, which in turn is waiting for another resource held by another waiting

process. If a process is unable to change its state indefinitely because the resources requested by it are being used by another waiting process, then the system is said to be in a deadlock.

5. What is hazard and mention its types?

Hazard is an unwanted switching transients.

1. Static 1 hazard: Output goes momentarily 0 when it should remain at 1
2. Static 0 hazard: Output goes momentarily 1 when it should remain at 0
3. Dynamic hazards: Output changes 3 or more times when it changes from 1 to 0 or 0 to 1

6. Define merger graph.

The merger graph is defined as follows. It contains the same number of vertices as the state table contains states. A line drawn between the two state vertices indicates each compatible state pair. It two states are incompatible no connecting line is drawn

7. Define state table.

For the design of sequential counters we have to relate present states and next states. The table, which represents the relationship between present states and next states, is called state table.

8. What are the steps for the design of asynchronous sequential circuit?

Construction of a primitive flow table from the problem statement is as follows,

(i)Primitive flow table is reduced by eliminating redundant states using the state reduction ii) State assignment is made (iii) The primitive flow table is realized using appropriate logic elements.

9. Define primitive flow table (Apr 2017)

It is defined as a flow table which has exactly one stable state for each row in the table. The design process begins with the construction of primitive flow table.

10. Explain about state Assignment in Synchronous circuit and asynchronous circuit.(Nov 2019)

In synchronous circuit, the state assignments are made with the objective of circuit reduction. In asynchronous circuits, the objective of state assignment is to avoid critical races.

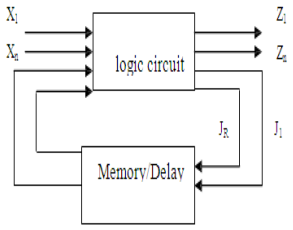
11. Write a short note on fundamental mode asynchronous circuit and pulse mode asynchronous circuit.((Nov 2015)

Fundamental mode circuit – Input signals change only one at a time and fixed

only when the clock is in stable condition.

Pulse mode circuit – Inputs are pulse triggered and pulse width is long enough for the circuit to responds to inputs.

12. Sketch the block diagram of an asynchronous sequential circuit? (Nov 2012) (Nov 2018)



13. What are state table and state diagram as applicable to sequential logic circuits?(Nov 2012)

The table which represents the relationship between present states and next states is called state table. State diagram is a pictorial representation of a behavior of a sequential circuit.

14. What is the difference between PROM AND EPROM ?(May 2013)

TERMS	**PROM**	**EPROM**
Expands to	Programmable Read Only Memory.	Erasable Programmable Read Only Memory.
Basic	The chip is one- time programmable only.	The chip is reprogrammable.
Cost	Inexpensive.	Costly as compare to PROM.
Construction	PROM is encased in a plastic covering.	A transparent quartz window covers EPROM.
Storage Capacity	High	Low comparatively.

15. Explain PROM. (Nov 2012) (Apr 2015)

PROM (Programmable Read Only Memory).It allows user to store data or program. PROMs use the fuses with material like nichrome and polycrystalline. The user can blow these fuses by passing around 20 to 50 mA of current for the period 5 to 20μs.The blowing of fuses is called programming of ROM. The PROMs are one time programmable. Once programmed, the information is stored permanent.

16. What is the difference between flow table and transition table? (May 2013)

Transition table is useful to analyze an asynchronous circuit from the circuit diagram.

Flow table is similar to a transition table except the states are represented by letter

symbols; it can also include the output values. Suitable to obtain the logic diagram from it. Flow table is similar to transition table, except that the internal states are symbolized with letters.

17. Define PLA. (Nov 2012)(Nov 2017) (Nov 2018)

PLA is Programmable Logic Array (PLA). The PLA is a PLD that consists of a programmable AND array and a programmable OR array.

18. What is PROM? (Nov 2015)(Apr 2015)

PROM- Programmable Read Only Memory is a device that contains Fixed AND and Programmable OR functions. IT contains fuses inact giving all 1`s in the stored bits and blown fuses by applying high voltage defining 0 states.

19. Mention the different types of hazard? (Nov 2019)

The different types of hazards are

(1)A static hazard in a logic network is a transient change of an output value which is supposed to remain fixed during the transition between two input states differing in the value of only one variable.

(i)Static-1 Hazard: the output is currently 1 and after the inputs change, the output momentarily changes to 0 before settling on 1.

(ii)Static-0 hazard: the output is currently 0 and after the inputs change, the output momentarily changes to 1 before settling on 0.

(2)Dynamic hazard is defined as a transient change which occurs three or more times at the output of logic circuit, when the output is supposed to change only once during the transient between two inputs which differ in the value of one variable.

20. What are the two types of asynchronous sequential circuits?(May 2016)

The two types of asynchronous sequential circuits are 1) Fundamental mode sequential circuit and 2) Pulse mode sequential circuits.

21.Why PAL is developed? (Apr 2018)

The PAL is programmable logic device with a fixed OR array and a programmable AND array. Because only the AND gate are programmable, the PAL is easier to program, but is not as flexible as the PLA.

22. State the difference between PROM, PLA and PAL. (May 2016)(Apr 2017)

PROM	**PLA**	**PAL**
PROM stands for Programmable read	PLA stands for Programmable Logic	PAL stands for Programmable Array

only memory	Array	Logic
One time programmable by user	Both AND and OR arrays are programmable	OR array is fixed and AND array is programmable
Its content cannot be erased	Costlier and complex than PAL and PROM's	Cheaper and simpler

23.List the basic configuration of three PLD's.(Nov 2019)

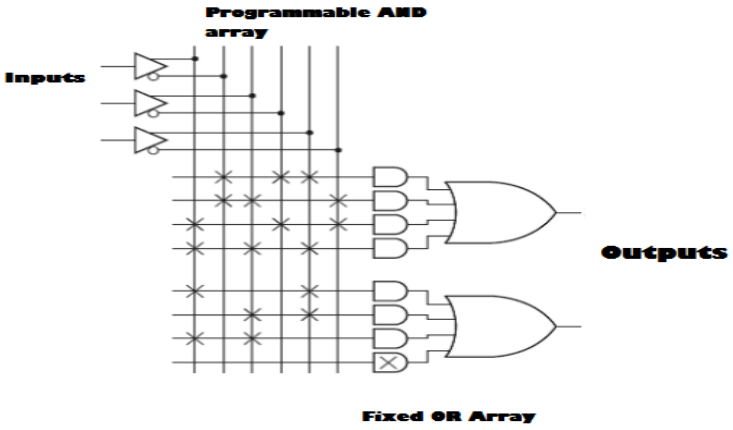
The three basic configuration of PLD's was given by

1. PROM(Programmable Read Only Memory)
2. PLA (Programmable Logic Array)
3. PAL (Programmable Array Logic)

24. Define metastable state. (Apr 2019)

Whenever there are setup and hold time violations in any flip-flop, it enters a state where its output is unpredictable: this state is known as metastable state (quasi stable state); at the end of metastable state, the flip-flop settles down to either '1' or '0'.

25. Draw the structure of PAL. (Apr 2019)



26.When does dynamic hazard occur in digital systems? (Nov 2020)

When the output changes several times while it should change from 1 to 0 or 0 to 1 only once, it is called dynamic hazard. Dynamic hazard occur when the output changes for two adjacent input combinations while changing, the output should change only once. But it may change three or more times in short intervals because of different delays in several paths. Dynamic hazards occur only in multilevel circuit.

27.Determine the size of the PROM required for implementing a dual 8 to 1 multiplexer with common selection inputs logic circuits.(Nov 2020)

The size of the PROM required for implementing an n-input, m-output combinational circuit is 2^n X m.For dual 8 to 1 multiplexer ,the number of input = (8+8+3 select input)=19 and number of output is 2

Size of PROM = 2^{19} X 2 = 512K X 2

PART-B

1. (i) Give the design procedure for Mealy and Moore machine.

   (ii) Give the design Procedure for asynchronous sequential circuit.

2. Design a gated latch circuit with two inputs, *G* (gate) and *D* (data), and one output *Q*. The gated latch is a memory element that accepts the value of *D* when *G* = 1 and retains this value after *G* goes to 0. Once *G* = 0, a change in *D* does not change the value of the output *Q*.

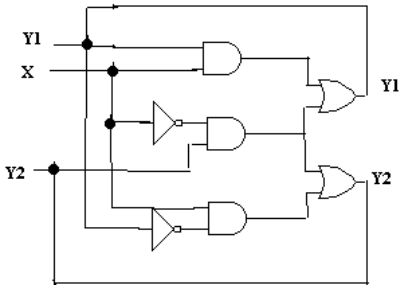
3. (i) What is PAL?

   (ii) Implement the boolean function using PAL: $Y_1=\sum m(1,3,5, 7)$ & $Y_2=\sum m(2,4)$ &

4. Explain the various types of hazards in sequential circuit design and the method sto eliminate them. Give suitable examples**. (Nov 2014)(Nov 2017)**

5. Describe with reasons, the effect of races in asynchronous sequential circuit design. Explain its types with illustrations. Show the method of race-free state assignments with examples**.(Nov 2019)**

6. Consider the following asynchronous sequential circuit and draw maps and transition table and state table**. (May 2013)**



7.(i)Sketch the transition table and state table for an asynchronous sequential circuit described by the following Boolean expressions:

$Y_1=X_1X_2+X_1Y_2+X_2Y_1$, $Y_1=X_2+X_2Y_1Y_2+X_1Y_1$, $Z=X_2+Y_1$ **(Nov 2012)**

(ii)Discuss the steps involved in the design of asynchronous sequential circuit with a suitable example.

8. (i) Design a combinational circuit which accepts three bit number and outputs a binary number equal to the square of the input number using PROM.

   (ii) Implement the Boolean function using PLA: $F_1(A,B,C)=\sum(0,1,2,4)$,

$F_2(A,B,C)=\sum(0,5,6,7)$.

9. Design a asynchronous sequential circuit (with detailed steps involved) that has 2 inputs x_1 and x_2 and one output z. The circuit is required to give an output z=1 when x_1=1, x_2=1 and x_1=1 being first. **(Nov 2015)**

10. Show how to program the fusible links to get a 4 bit gray code from the binary inputs using PLA and PAL and compare the design requirements with PROM. **(Nov 2015)**

11. Design an asynchronous sequential circuit that has two inputs X_2 and X_1 and one output Z. The circuit is required to give an output whenever the input sequence (0,0),(0,1) and (1,1) received but only in that order**.(May 2016)**

12. (i) what are static-0 and static-1 hazards? Explain the removal of hazards using hazard covers in k-map. (ii) Explain cycles and races in asynchronous sequential circuits**. (Nov 2018)(Nov 2019)**

13. (i) What are transition table and flow table? Give suitable examples**.(May 2016)**(ii) Implement the following function using PLA and PAL: $F(X,Y,Z)=\sum m(0,1,3,5,7)$**(May 2016) (Apr 2017)**

14. (i) Implement the following function using PLA: $F(x,y,z)=\sum m(1,2,4,6)$**(Apr 2017)**

(ii)For the given boolean function, obtain the hazard free circuit

$F(A,B,C,D)=\sum m(1,3,6,7,13,15)$ **(Apr 2015) (Apr 2017)**

15. Design an asynchronous sequential circuit that has two inputs X_2 and X_1 and one output Z. When X_1 =0,the output Z is 0.The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1.The output Z will remain 1 until X_1 returns to 0**.(Apr 2015)**

16. Write short notes on PLA and PAL. **(Nov 2017)**

17. Explain the concept of PROM, EPROM and EEPROM in detail. **(Apr 2018)**

18. Explain the concept of bipolar RAM cel with suitable diagram. **(Apr 2018)**

19. Discuss the operation of SR latch with NOR and NAND gates analysis. **(Nov 2018)**

20. Design an asynchronous sequential circuit that has two inputs X2 and X1 and one output Z. Initially both inputs are equal to zero. When X_1 or X_2 =1,the output Z is 1.When the second input also becomes 1 the output changes to 0.The output stays at 0 until the circuit goes back to the initial state **(Nov 2017)**

21. Implement the functions $F_1(X, Y, Z)= \sum(1, 2, 4, 5)$, $F_3(X, Y, Z)= \sum(0, 1, 3,4)$ and $F_2(X, Y, Z)= \sum(2, 3, 6, 7)$ using a single PROM grid. **(Apr 2019)**

22. (i) Differentiate PAL and PLA implementations with the help of the same example F(a, b, c)= ∑(0, 1, 3, 4, 6, 7).

(ii) Explain the structure of CPLD with the help of block diagram.**(Nov 2020)**

23. You have two two-bit binary numbers a1a0 and B1B0. Design a PLA device to implement a magnitude comparator to produce outputs for a1a0 being 'equal to', 'not equal to', 'less than' and 'greater than' B1B0. **(Nov 2020)**

24. Implement the following function using PLA and PAL :F1 (A,B,C)= Σm(3,5,6,7) and F2 (A,B,C)= Σm(0,4,2,7) **(Nov 2019)**

UNIT V- VHDL

PART A

1. Write some of the Low Level Languages and High Level Languages?

i) Low Level Languages-ABEL

ii) CUPL

iii) PALASM High Level Languages-VHDL and iv) VERILOG

2. What are the types of simulation? Or what are the different modeling techniques used to describe a module? (Nov 2012)

Behavioral simulation, Functional simulation, Logic or gate level simulation, Switch level simulation, Transistor level simulation

3. What is static timing analysis?

One class of simulators employed timing analysis that analysis logic in a static manner, computing the delay timing for each path. This is called static timing analysis because it does not required the creation of set of test vectors.

4. Define gate level simulation.

It can be also used to check the timing performance of an ASIC. In a gate level simulation a logic gate or logic cell is treated as a black box modeled by a function whose variable are single inputs. The function also mode the delay through the logic cell setting all the delay value to unit value is the equivalent of functional simulation.

5. What is the purpose of VHDL programming? Or what is the need for VHDL? (May 2013)

Very high speed integrated circuit hardware description language. It is a language for describing a hardware, which has to be readable for machines and humans at the same time & it structured and comprehensible code, so that the source code can serve as a kind of specification document. Thus it is used for studying digital logic circuits and

testing its functions.

6. What are sequential and concurrent statements?

Sequential statements are executed one after other, like in software programming languages. The order of assignment must be considered when sequential statements are used. In VHDL, it is used in behavioral description of the design. Statements within the "process" unit are executed sequentially. Concurrent statements are active continuously. So the order of the statements is not relevant. Concurrent statements are especially suited model the parallelism of hardware. In VHDL, all statements except within "process" are executed concurrently.

7. What are the main components of a VHDL description?

The main components of VHDL descriptions are,

1. Package (optional)
2. Entity
3. Architecture
4. Configuration**.**

8. What is entity?

Entity gives the specification of input/output signals to external circuitry. It gives interfacing

between device and the other peripherals. An entity usually has one or more ports, which are analogous to the pins on a schematic symbol. All information must flow into and out of the entity through the ports. Each port must contain name, data flow direction and type.

9. Give the classification of data types supported by VHDL.

The VHDL data types can be broadly classified into following five data types:

Scalar types:

The scalar types include numeric data types and enumerated data types. The numeric types consist of integer, floating point (real) and physical types. Bit, Boolean and character are all enumerated types.

Composite types: Array and record types are composite data types. The values of these types are collection of their elements**.**

Access types: They are pointers, they provides access to objects of a given data type.

File type: They provide access to object that contain a sequence of values of given type.

Other types: They include the data types provided by the several external libraries.

10. Give the syntax for VHDL entity declaration?

The syntax of a VHDL entity declaration is as shown below:

Entity entity_name is

Port (signal_names: mode signal_type; Signal_names: mode signal_type);

end entity name;

11. What is architecture?

Architecture specifies behavior, functionality, interconnections or relationship between inputs and outputs. It is the actual description of the design. An architecture consists of two portions: architecture declaration and architecture body.

12. List the internal details of an entity specified by architecture body.

An architecture body specifies following internal details of an entity: (i) As a set of concurrent assignment statements to represent dataflow. (ii) As a set of interconnected components to represent structure. (iii) As a set of sequential assignment statement to represent behavior.

13. Give the syntax for VHDL architecture declaration.

The syntax for architecture is given below:

Architecture architecture_name of entity_name is

Begin

Concurrent statements; Sequential statements;

End architecture_name;

14. What is the use of configuration declaration?

Configuration declarations may associate particular design entities to component instances (unique references to lower level components) in a hierarical design or to associate a particular architecture to an entity.

15. What is the need of package declaration?

There are some declarations which are common across many design units. A package is a convenient mechanism to store and share such declarations. A set of declarations contained in a package declaration may be shared by many design units. It defines items that can be made visible to other design units.

16. What is subprogram?

A subprogram defines a sequential algorithm that performs particular task. Two types of subprograms are used in VHDL Procedures and functions. Procedures and

function in VHDL are directly analogous to functions and procedures in a high level programming language such as C or Pascal.

17. List the different types of operators supported by VHDL? (Nov 2012)

The different operators supported by VHDL are, Logical operators, Arithmetic operators, Relational operators and shift operators.

18. The 'module' is the basic building block of VHDL. What are the different modeling techniques used to describe a module? (Nov 2012)

- Structural modeling,
- Data flow modeling,
- Behavioral modeling.

19.Write behavioral model of D flip flop. (Nov 2016) (Apr 2015)

```
Library ieee;
Use ieee.std_logic_1164.all;
Entity dff is
Port (D,clk,rst:instd_logic; Q: out std_logic);
End dff;
Architecture behave of dff is
Begin
Process (rst,clk)
Begin
If rst='0' then Q<='0';
else
clock'event and clk='1' then Q<=D;
End If:
End process;
End behave;
```

20.What is a package in VHDL?(Apr 2015)

A VHDL package contains subprograms, constant definitions, and/or type definitions to be used throughout one or more design units. Each package comprises a "declaration section", in which the available (i.e. exportable) subprograms, constants, and types are declared, and a "package body", in which the subprogram implementations are defined, along with any internally-used constants and types.

21.Write a VHDL code for 2:1 MUX using Behavioral model (May 2016)(Apr 2017)

```
Library ieee;
Use ieee.std_logic_1164.all; Entity mux2_1 is
Port (a,b,sel:instd_logic; c: out std_logic);
End mux2_1;
Architecture muxarch of mux2_1 is
Begin
Process (a,b,sel) Begin
If s='0' then c<=a;else s='1' then c<=b; End If;End process;
End muxarch;
```

22.State the advantage of package declaration over component declaration.

Package declaration is used to declare components, types, constants, functions and so on.

Declared Packages will be shared by many design units.

Component declaration declares the name of the entity and interface of a component which is used by the design unit. Declared Component will be used by the corresponding design unit.

23.Write the VHDL code for a logical gate which gives output only when both the inputs are high. (Nov 2016)

The logical gate which gives output only when both the inputs are high is AND gate. The code is as follows,

```
entity andgate is
    Port( a, b:in std_logic; c: out std_logic);
end andgate;
architecture behavi of andgate is
begin
C<=a and b;
end behave;
```

24.What is data modeling in VHDL? Give its basic mechanism. (May 2016)

- "Entity" describes the external view of a component.
- "Architecture" describes the internal behavior and/or structure of the component

Example: Half Adder Code

```
entity Half_Adder is
port (X, Y : in STD_LOGIC;
Sum, Cout : out STD_LOGIC);
end;
architecture Behave of Half_Adder is
begin
Sum <= X xor Y; -- use formals from entity
Cout <= X and Y; -- “operators” are not “gates”
end Behave;
```

25.List out the logical operator present in VHDL. (Nov 2015)

SYMBOL	OPERATION
^	Bitwise XOR
~	Bitwise NOT
&	Bitwise AND
|	Bitwise OR
&&	Logical AND
||	Logical OR
!	Logical NOT

26. Define Modularity. (Nov 2017)

Modularity allows the partitioning of big functional blocks into smaller units and to group closely related parts in self-contained subblocks, so called modules.

26. Give the Syntax for Package declaration and Package Body in VHDL (Apr 2017)

Package Body Declaration:

```
package body package_name is
    subprogram bodies
    complete constant declarations
    subprogram declarations
    type and subtype declarations
    file and alias declarations
    use clauses
end package_name;
```

Package Declaration:

package package_name **is**

package_declarations

end package package_name;

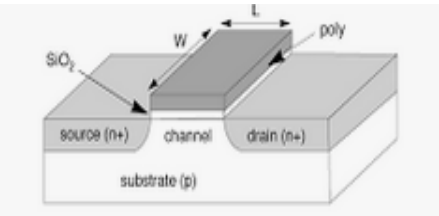
27. Infer the concept of switch level modeling. (Apr 2018)

The switch level of modeling provides a level of abstraction between the logic and analog-transistor levels of abstraction, describing the interconnection of transmission gates which are abstractions of individual MOS and CMOS transistors.

28. Define Cache memory (Apr 2018)

Cache memory, also called CPU memory, is high-speed static random access memory (SRAM) that a computer microprocessor can access more quickly than it can access regular random access memory (RAM). This memory is typically integrated directly into the CPU chip or placed on a separate chip that has a separate bus interconnect with the CPU. The computer processor can access this information quickly from the cache rather than having to get it from computer's main memory. Fast access to these instructions increases the overall speed of the program.

29. Draw the basic structure of MOS transistor. (Nov 2018)



30. List the languages that are combined together to get VHDL language. (Nov 2019)

1. Sequential language
2. Concurrent language
3. Net- List language
4. Waveform generation language

31. Explain the T Base and T Low predefined attributes (Nov 2019)

An attribute gives extra information about a specific part of a VHDL description. Predefined attributes can be constants, functions or signals. In the VHDL standard a set of predefined attributes is defined

T'BASE is the base type of the type T

T'LOW is the lowest value of type T.

32. State the purpose of Test bench. (Apr 2019)

Test Bench Mainly used for:

(i) Generating stimulus for simulation.

(ii) Applying the stimulus to the entity under test and to collect the output.

(iii) Comparing obtained output with expected output.

33. Write a VHDL program for an EX-NOR gate using behavioral coding. (Apr 2019)

VHDL Program:

```
library IEEE;
Use IEEE.STD_LOGIC_1164.ALL;
Use IEEE.STD_LOGIC_ARITH.ALL;
Use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity exnorgate is
   Port(a,b: in std_logic; c: out std_logic);
end exnorgate;
architecture Behavioral of exnorgate is
begin
c<=a xnor b;
end Behavioral;
```

34. Explain in words and write HDL statements for the operations specified by the following register transfer notation : if (S1 = 1) then (R0 ← R1) else if (S2 = 1) then (R0 ← R2). (Nov 2020)

If S1=1 , transfer the contents of the register R1 to R0

If S2=1, transfer the contents of the register R2 to R0

35. What is the use of repeat statement in verilog HDL ? (Nov 2020)

A repeat statement in Verilog HDL will repeat a block of code some defined number of times. It is very similar to a for loop, except that a repeat loop's index can never be used inside the loop. Repeat loops just blindly run the code as many times as you specify.

PART-B

1.What is a hardware description language ? What are the requirements of a good HDL ? Briefly describe the salient features of VHDL and verilog.(8)

ii) Write the VHDL code for four bit adder circuit.(5)

2.Explain the digital system design flow sequence with the help of a flowchart. **(Nov 2014)**

3.Explain the concept of Behavioral modeling and Structural modeling in VHDL. Take example of Full Adder design for both and write the coding**.(Nov**

2014)(Nov 2015)(Apr 2015) (Nov 2016)(Nov 2017)

4.Write a VHDL program to implement SR latch and JK-flip flop using behavioral model**.(Nov 2017)**

5. (i) Briefly discuss the use of Packages in VHDL. **(Nov 2012)**

(ii)Write a VHDL code that implements an 8:1 multiplexer.

6.Write VHDL for four bit binary counter with parallel load and explain. **(Apr 2013)**

7. Write VHDL code for JK master flip-flops as structural element and also write code for 4 bit asynchronous counter.

8. Explain test bench with suitable example.

9. Explain in details the RTL design procedure. **(Nov 2015)**

10. Write a VHDL Program for 1 to 4 DMUX using data flow modeling. **(Nov 2015)**

11. Write the VHDL code to realize 3-bit Gray code counter using case statement**.(Nov 2019)**

12. (i) Write short notes on built in operators used in VHDL programming. **Nov 2016)**

(ii) Write VHDL coding for 4 × 1 MUX

13. Discuss briefly the operators and packages in VHDL.**(Nov 2019)**

14. (i)Explain functions and subprograms with suitable examples.

(ii)Write the VHDL code to realize a 4 bit parallel binary adder with structural modeling and write the test bench to verify is functionality**.(May 2016)**

15. Design a 4 bit code converter which converts given binary code into a code in which the adjacent number differs by only 1 by the preceding number. Also, develop VHDL coding for the above mentioned code converter**. (Nov 2016)**

16. (i)Write a VHDL code for a 4-bit universal shift register. **(Nov 2014)**

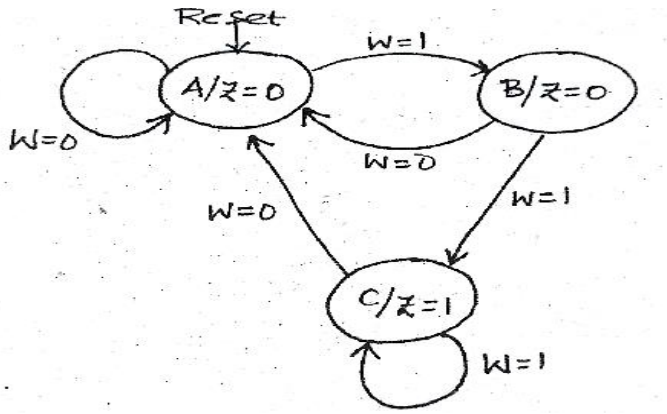
(ii) Write HDL for (a) four bit adder (b) Mod 8 Counter. **(Apr 2013)**

17. (i) Design a 3 bit magnitude comparator and write the VHDL code to realize it using structural model

(ii) Design a 4 × 4 Array multiplier and write the VHDL code to realise it using structural model. **(Apr 2017)**

18. Write a VHDL code to realize a half adder using behavioral modeling and structural modeling. **(Nov 2018)**

19. Write the VHDL code for the given state diagram, using behavioral modeling.



Design it using one-hot state assignment and implement it using Programmable Array Logic (PAL). **(Apr 2017)**

20. Draw the circuit of CMOS AND gate and explain it's operation. Also implement it using VHDL. **(Apr 2018)**

21. (i) Draw the VLSI design flow chart used for IC design and fabrication.

(ii) Write down a VHDL code for 8×1 Demultiplexer. **(Apr 2019)**

22. (i) Illustrate the two approaches used in VHDL coding with full adder design as your example.

(ii) What are components in VHDL? Show step-by-step how a NOR gate component can be created and added in the library. **(Apr 2019)**

23. i) Explain in detail about ASMD chart for digital system design. (5)

ii) Explain in detail about ASM block with an example.(8) **(Nov 2020)**