Unit-1 IC Fabrication

EE8451 - Linear Integrated Circuits and Applications

IC classification, fundaments of monolithic IC technology, epitaxial growth, masking and etching, diffusion of impurities. Realisation of monolithic ICs and packaging. Fabrication of diodes, capacitance, resistance, FETs and PV cell.

Classification of ICs

* Micro Electronic revolution

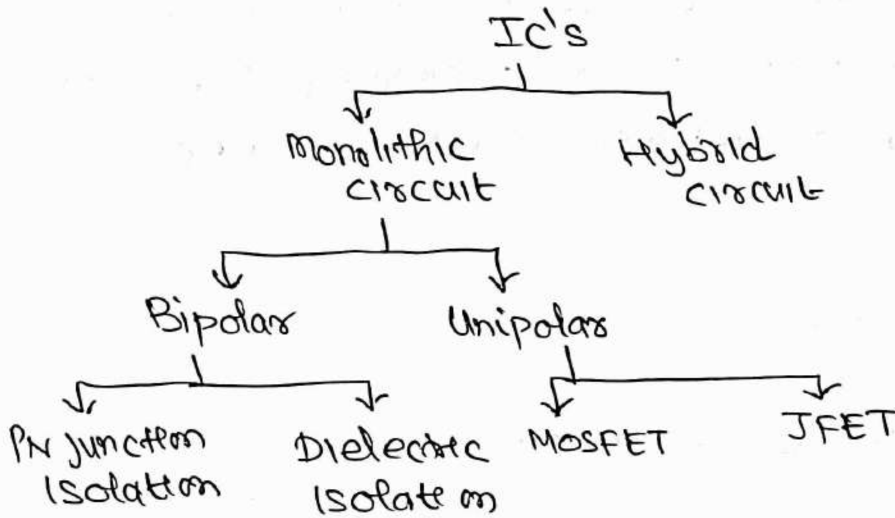
* Integrated circuits - Many Components can be fabricated

ICs - miniature, low cost electronic circuit consisting of Active and passive Components that are irreparably Joined together on a single chip of Silicon

Advantages

* Miniature in size, hence increased equipment density
* cost reduction due to batch processing
* Increased system reliability due to elimination of soldered joints
* reduction in power consumption
* Increased operating speed
* Improved functional performance
* Matched devices

Integrated circuits (IC's)



IC chip size and circuit Complexity

* Until 1950's, Electronic device technology was dominated by Vacuum tube.
* Invention of Transistor (1947) was followed by development of IC.
* IC – 1960 – Introduction – Texas Instruments, Fairchild semiconductor

Small Scale Integration (SSI) — 3 to 30 gates / chip, 100 transistor / chip, logic gate, flip-flops

Medium Scale Integration (MSI) — 3 to 300 gates, 100 to 100 transistor, Counters, multiplexers

Large Scale Integration (LSI) 300 to 3000 gates
1000 - 20,000 transistors
(8 Bit μp, RAM, ROM)

Very Large scale Integration (VLSI) more than 3000/gates
20,000-10,00,000 transistors
[16 & 32 Bit μp's)

Ultra Large Scale Integration (ULSI) $10^6 - 10^7$ transistor
(smart sensors)

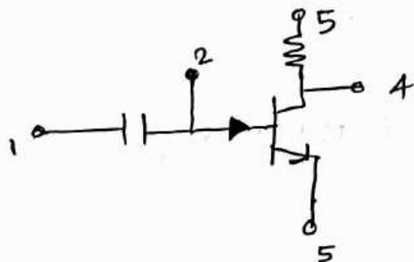
Giant - Scale Integration (GSI) $>10^7$ transistor/chip

Fundamentals of monolithic IC technology

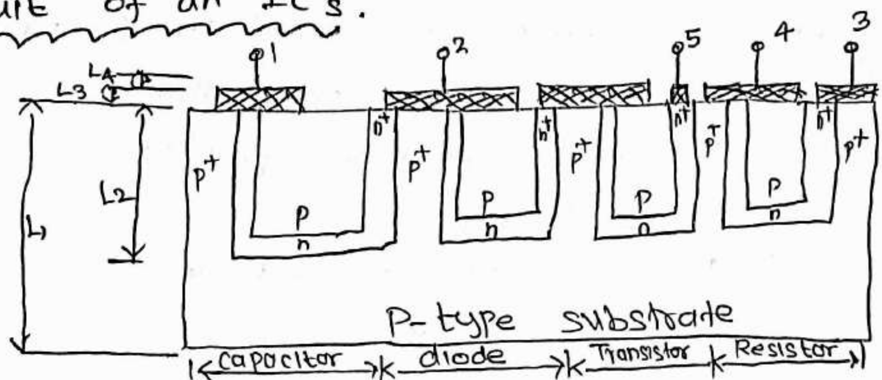
* A monolithic circuit means circuit fabricated from a single stone or single crystal.

* monolithic Greek word Mono - single
lithos - stone

* major advantage: Reducing the cost of production of electronic circuits.



Typical circuit of an IC's.



Layer No:1 (~400 μm) - p type silicon substrate upon which IC's are fabricated

Layer No:2 (~5-25 μm) - thin n-type material grown as a single crystal extension of substrate using epitaxial deposition technique. All active & passive components are fabricated within layer using selective diffusion of impurities

Layer No:3 (0.02-2 μm) Very thin SiO_2 layer - preventing diffusion of impurities

Layer No: 4 (~1 μm) aluminium layer - obtaing interconnection b/w components

Basic planar process of Monolithic IC

1. Silicon wafer preparation
2. Epitaxial growth (SEOP DIIMA)
3. Oxidation
4. photolithography
5. Diffusion
6. Ion Implantation
7. Isolation technique
8. Metallization
9. Assembly processing and packaging

① Silicon wafer preparation

following steps are used in preparation of Si-wafers

1. crystal growth and doping
2. Ingot trimming and grinding
3. Ingot slicing
4. wafer polishing and etching
5. wafer cleaning

* Czochralski crystal growth - most commonly used process for producing single crystal silicon ingot.

* Poly crystalline silicon + amount of dopant } → Put in a quartz crucible and placed in furnace.
* Heated to 1420°C ; greater than silicon melting point.
* Small single crystal rod of silicon called seed crystal. seed crystal is dipped into the silicon melt and slowly pulled out

* It brings with it a solidified mass of silicon with the same crystalline structure as that of seed crystal.

* During the crystal pulling process, seed crystal and crucible are rotated in opposite direction in order to produce ingot of circular cross section

* Diameter of ingot - controlled by - pulling rate, melted temperature
→ crystal growth

→

* Ingot diameter 10 to 15 cm
Ingot length 100 cm
* After cutoff ingot surface is ground to produce an exact diameter.
* Ingot - tested for resistivity and perfection
* the portion failed in the above list is also cut - called as ingot trimming

* Ingot - surface grinding - carried out with help of lathe like diamond tool.
→ trimming + grinding

→

* with a reference plane, the ingot is sliced by stainless steel saw blade with industrial diamonds embedded into the inner diameter cutting edge

→ slicing

→ * After cutting the ingot, silicon wafers will undergo number of polishing to provide highly polished finish surface.

* Before etching process, two sided mechanical lapping process is carried out to bring the wafer with uniform flatness.

* Hydrofluoric + acetic + nitric acid → acidic/chemical etching

* potassium hydroxide/sodium hydroxide → alkaline etching

→ polishing and etching

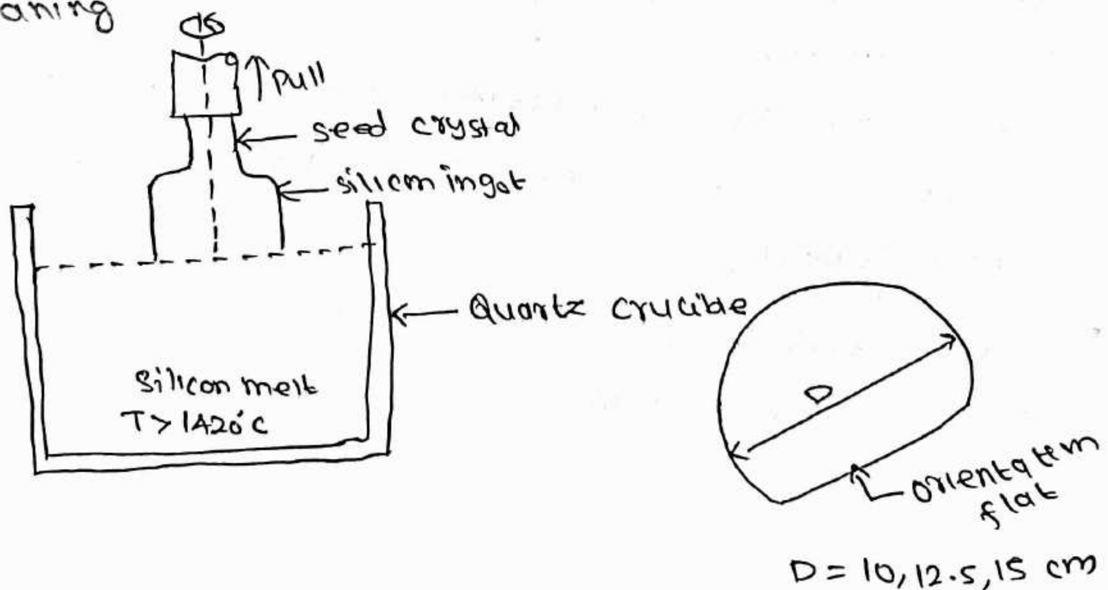
→

* silicon wafers are cleaned using chemicals to remove metallic impurities. then rinsed in water to deionize.

* finally, the wafers are thoroughly rinsed & dried.

* Each silicon wafer contain several hundred rectangular chip, each containing a comple IC having side of 10 to 1mm.

→ cleaning



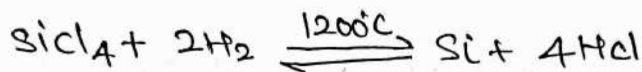
② Epitaxial growth

* epitaxy = Greek work

epi : upon   teinon: arranged

arranging atoms in a single crystal fashion upon a single crystal substrate. So resulting layer is an extension of the substrate crystal structure.

* Basic chemical reaction used for epitaxial growth of pure silicon : Hydrogen reduction of silicon tetrachloride.



$$SiCl_4 + 2H_2 \underset{}{\overset{1200°C}{\rightleftharpoons}} Si + 4HCl$$

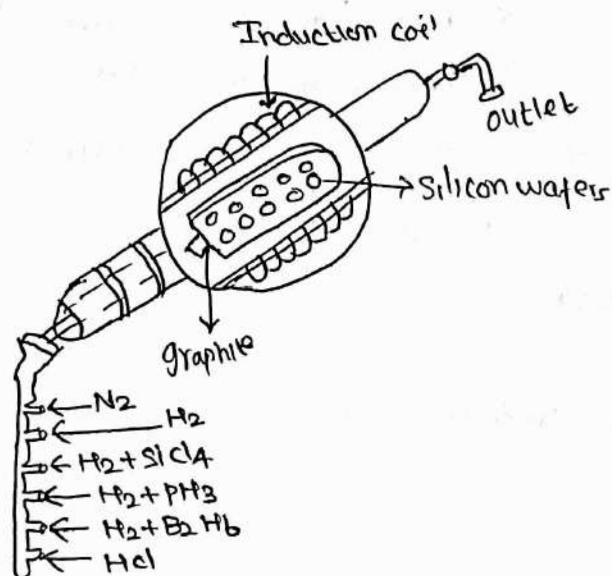
* epitaxial growth/films with specific impurity concentration are required.

PH_3 : phosphine n type] doping into the silicon
bi borane B_2H_6 p type] tetrachloride hydrogen gas stream.

* process carried out in a reaction chamber - consisting of a long cyclindrical quartz tube encircled by an RF induction coil.

* Silicon wafer placed in a rectangular graphite rod-boat. this boat placed in a reaction chamber, where graphite is heated inductively to 1200° c.

* Various gases required for growth of desired epitaxial layer are introduced in the system through a control sole



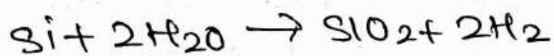
③ Oxidation

* SiO_2 → property of preventing the diffusion of almost all impurities through it.

(a) SiO_2 → extremely hard protective coating & is unaffected by almost all reagents except hydrofluoric acid.

(b) By selective etching SiO_2, diffusion of impurities thru carefully defined windows in the SiO_2 can be accomplished to fabricate various components

* Silicon wafers → stacked up in a quartz boat; then immersed/inserted into quartz furnace tube. Si wafers are raised to high temperature 950°C to 1115°C



$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

* This is called thermal oxidation. bcoz high temperature is used to grow the oxide layer.
  thickness governed by time, temp, moisture content

④ Photolithography

* By photolithography, possible to produce microscopically small circuit and device pattern on Si-wafers.

* Conventional method – "UV light" exposure device dimension: 2 µm

* Latest method – "X-ray"/electron beam technique dimension < 1 µm

Photolithography involve two process namely

(i) Making of a photographic mask
(ii) Photo etching.

(i) Preparation of initial work
(ii) Reduction

Preparation of inital work

* Initial layout of an IC is normally done at a scale, several hundred times larger than the final dimension of finished monolithic circuit

* This because, for a tiny chip larger the art work more accurate is the final work.

* Initial layout is then decomposed into several mask layers, each corresponding to a process step in the fabrication schedule.

* Photographic process art work should not contain any line drawings but must be of alternate clear and opaque regions.

* done by use of clear mylar coated with a sheet of red photographically opaque. mylar.

* art work done by precision drafting machine called coordinatograph.

* the final image also must be repeated many times in a matrix array. so that many IC's will be produced in one process.

photo Etching

* used for removal of SiO_2 from desired regions so that the desired impurities can be diffused.

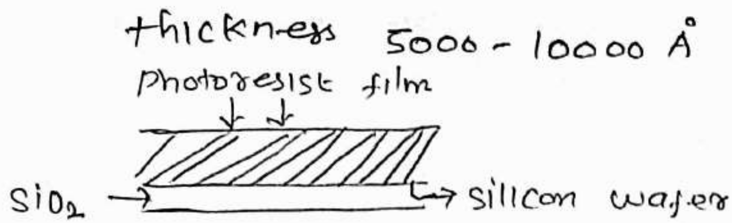
* wet etching process → chemical reagents used are in liquid form

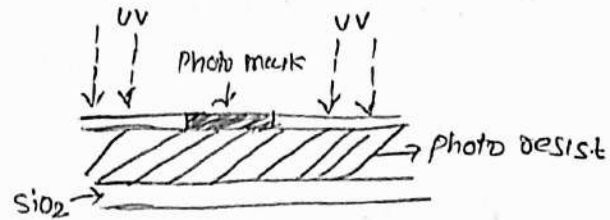
New process → plasma etching.

Advantage of dry etching: possible to achieve smaller line openings $\leq 1\mu m$
(μ^* - micro)

Step A : wafer → coated → film of photosensitive emulsion
(Kodak photoresist KPR)

thickness 5000 - 10000 Å

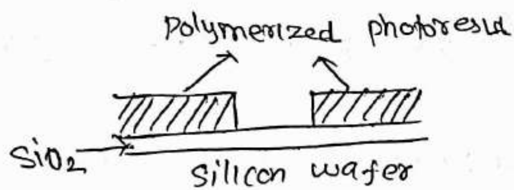


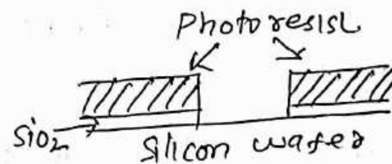


Step B : mask negative of the desired pattern as prepared by steps described earlier is placed over the photoresist coated wafer.

Now expose the wafer to UV light, so KPR becomes polymerized beneath the transparent region of mask

Step C: Mask is then removed, wafer developed using chemical which dissolves the unexposed/unpolymerized regions. on the photoresist and leaves the pattern.





Step D: polymerized photoresist is next fixed/cured, so that it becomes immune to etchants.

Chip → immersed in etching solution of HCl, remove the SiO_2 from the area's which are not protected by KPR. after diffusion of impurities photoresist is removed with a chemical solvent & mechanical abrasion.

* UV photo lithography
(conventional method)

* X-ray and electron beam lithography
(latest technique)

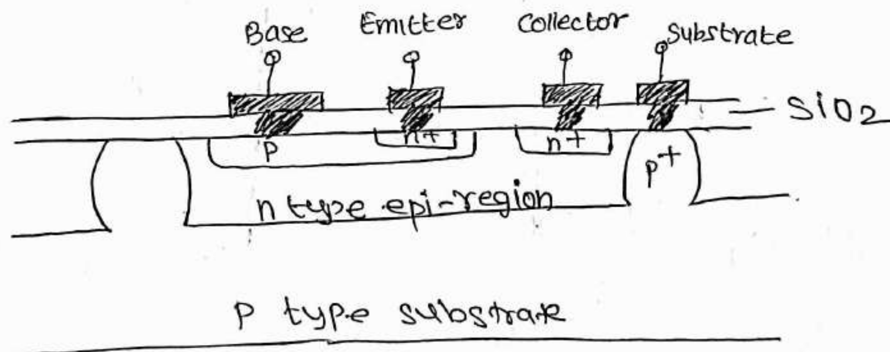
⑤ Diffusion

* This process uses a high temperature furnace having a flat temperature profile over a useful length.
* quartz boat containing about 20 cleaned wafers is pushed into the hot zone with temperature maintained at about 1000° C
* Impurities diffused are rarely used in their elemental form

Boron oxide B_2O_3] → Sources of Boron
Boron chloride BCl_3]

P_2O_5 Phosphrous pentaxide ; $POCl_3$ phosphrous oxychloride] → Sources of Phosphrous

* Carrier gas, such as dry oxygen/nitrogen is normally used for sweeping the impurity to the high temperature zone.
* depth of diffusion depends on time of diffusion.
* diffusion takes places both laterally as well as vertically.



⑥ Ion Implantation

* Another technique used to introduce impurities into a silicon wafer.
* The silicon wafers are placed in a vaccum chamber and are scanned by a beam of high energy dopant ions.
* These ions are acclerated by energies b/w 20 kV to 250kV.

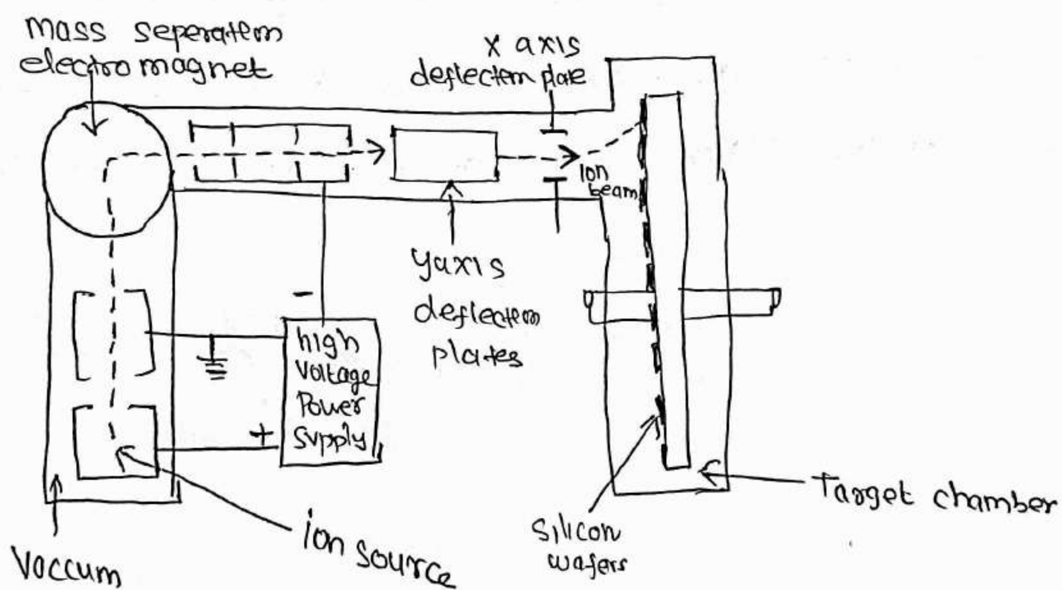
* the ions strike the silicon wafers, they penetrate some small distance into the wafer.

* depth of penetration increases with increasing the acclerating voltage.

* Two major advantages of ion implantation

  (a) performed at low temperature. Therefore previously diffused regions have a lesser tendency for lateral spreading

  (b) In diffusion process, temperature has to be controlled over a large area inside the oven, whereas here, acclerating potential & Beam current are electrically controlled from outside.



⑦ Isolation technique

* To provide electrical isolation b/w different components and interconnections, the isolation technique are used

  (a) p-n junction isolation

  (b) Dielectric isolation.

7.1 P-n junction Isolation

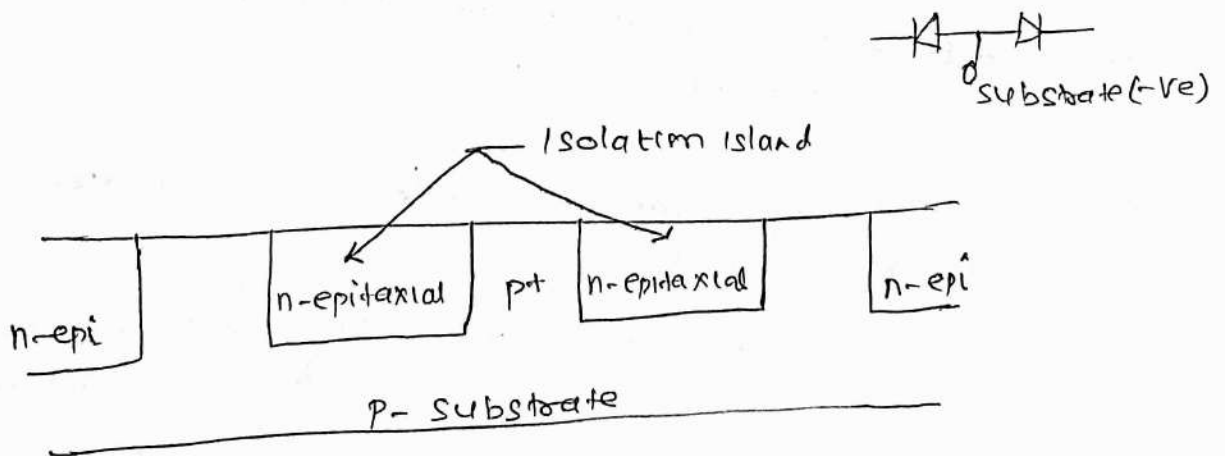
* Here p^+ type impurities are selectively diffused into the n-type epitaxial layer. so as to reach p-type substrate.

* This produce islands surrounded by p-type moats. It can be seen that regions are seperated by two back to back PN junction diode.

* If the p-type substrate material is held at the most negative potential in the circuit, the diodes will be reverse biased providing electric isolation b/w these islands.

* To prevent the depletion region of the reverse bias, always p+ is higher than the p-substrate.

* The presences of a transistion capacitance at the isolating pn junctions, resulting in an inevitable capacitor coupling between the components and the substrate. called as parasitic capacitance limit the performance of the circuit at high frequencies.

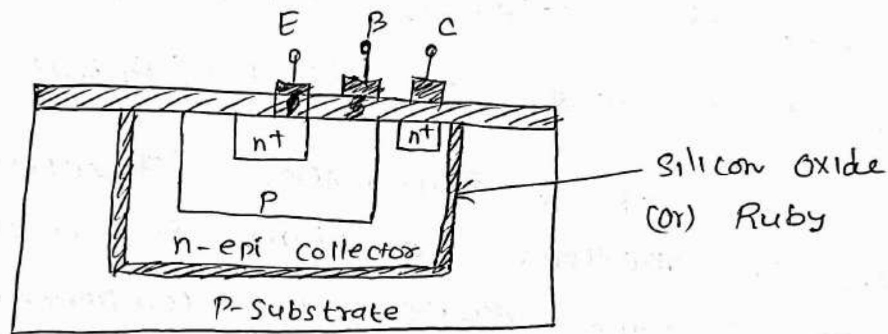


7.2 Dielectric isolation

* layer of solid dielectric such as silicon dioxide or ruby completely surrounds each component, thereby producing isolation both electrical and physical.

* Very thick layer with capacitance is negligible. Also possible to fabricate both npn and pnp transistor with same silicon substrate.

* more expensive bcoz of additional steps requirement.

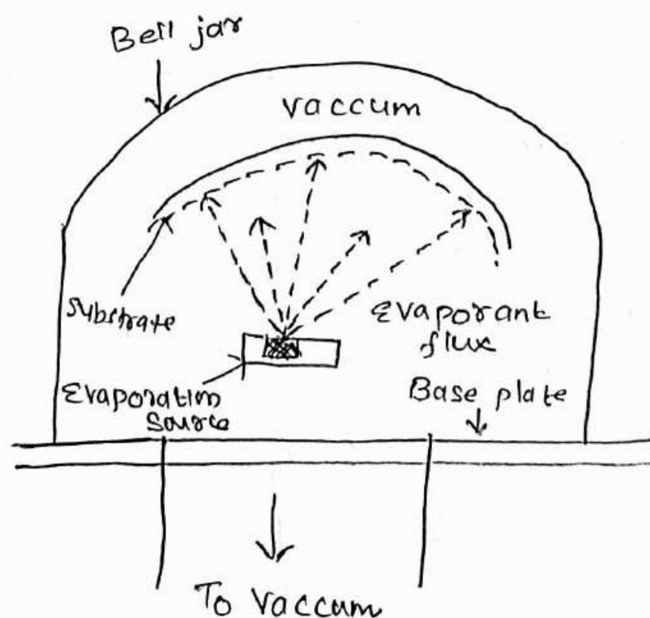


(8) Metallization

* purpose of this process to produce a thin metal film layer that will serve to make interconnections of various components on the chip.

* Aluminium is used for metallization purpose bcoz it has following advantage.
  (a) Relatively good conductor
  (b) easy to deposit aluminium films using vaccum deposition
  (c) make good mechanical bond with silicon
  (d) offer low resistance

* Process takes place in a Vaccum evaporation chamber.
* chamber pressure is reduced to the range of about 10^{-6} to 10^{-7} torr.
* material to be evaporated is placed in a resistance heated tungsten coil or basket.
* Very high power density electron beam is focussed at the surface of the material to be evaporated
* this heats up the material at very high temperature and its starts vapourising. Vapours travels in a straight line path.
* Evaporated material/molecules hit the substrate and form a thin film coating.
* The metallization is done, the film is patterend to produce the required inter connection and bonding pad configuration.



⑨ Assembly processing and packaging

* Each of the wafer processed contains several hundred of chips, each being a complete circuit.

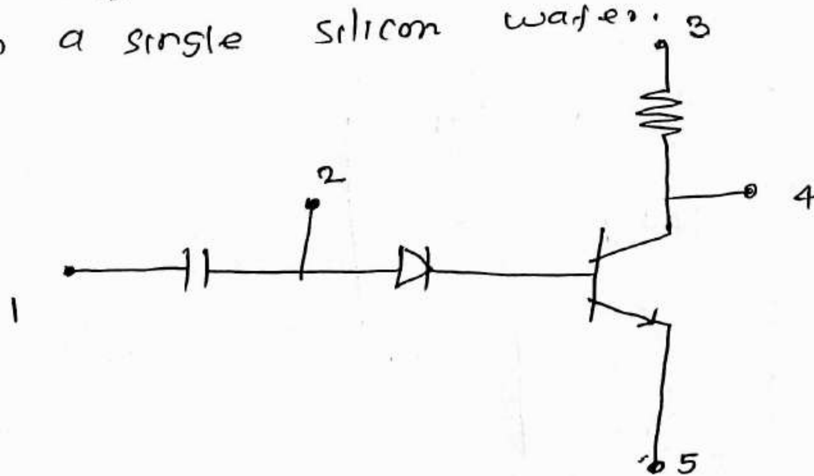
* Common method called scribing and cleaving used to for seperation, make use of a diamond tipped tool to cut lines into the surface of the wafer along the rectangular grid separating the individual chips.

* Metal can package - 8, 10 or 12 leads
* Ceramic flat package] 8, 14, 16 leads
* Dual-in-line package] 24, 36 or 42 leads

* Most of general purpose ICs are dual-in-line plastic packages due to economy.

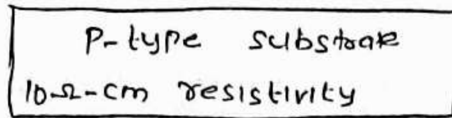
Realisation of monolithic ICs

* monolithic ICs can be obtained by fabricating a circuit in a single silicon wafer..



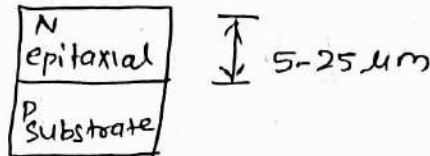
Step 1 : wafer preparation

P type silicon wafer



thickness : ~400 μm
10 cm diameter

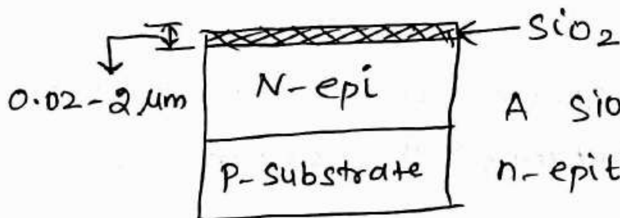
Step 2 : Epitaxial growth



n type epitaxial layer - ultimately becomes the collector region of the transistor / an element of diode & diffused capacitor associated with the circuit.

resistivity : 0.1 to 0.5 Ω-cm

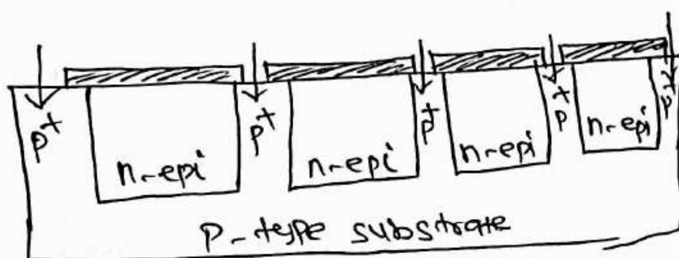
Step 3 : oxidation



A SiO_2 layer is grown on the n-epitaxial layer.

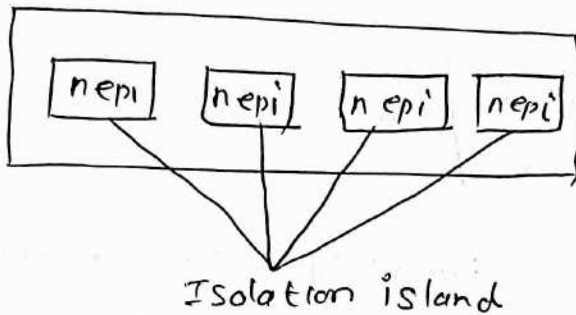
Step 4 : Isolation diffusion

A component to be fabricated; so four islands which are isolated. For this SiO_2 is removed from five different places using photolithographic technique.



* Now wafer → subjected to heavy p-type difussion for a long time interval. So p-impurities penetrate the N-type epitaxial layer and reaches the p-type substrate.

* Area under SiO_2 are n-type islands, that are surrounded by p-type substrate/moats.



* Keep, the PN junctions b/w the isolation islands at reverse biased condition (p-type substrate is held at negative potential wrt n-type islands), the islands are electrically isolated from each other.

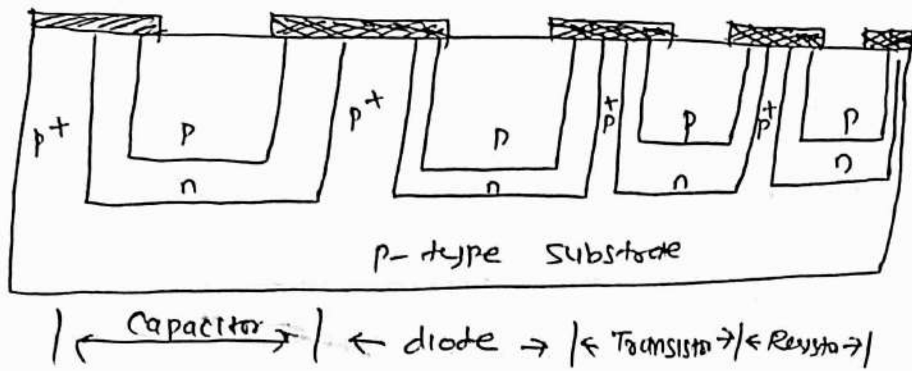
Step 5: Base diffusion

* New layer of SiO_2 is grown over the entire wafer and new pattern of openings is formed by photolithography

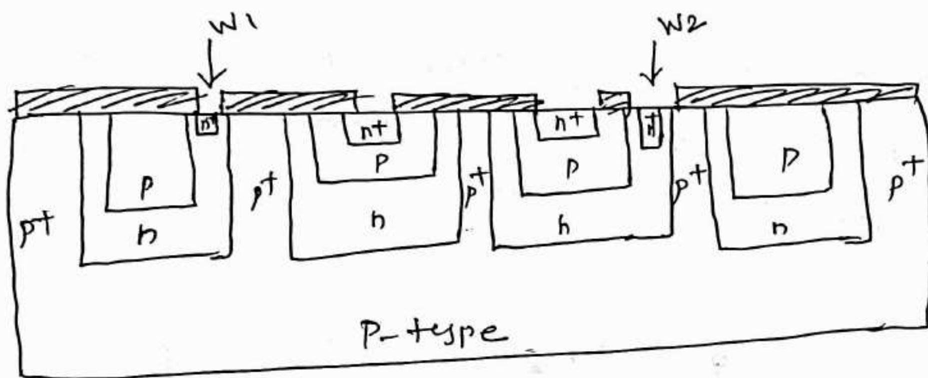
* p-type impurities such as boron are diffused through the openings into the island of n-type epitaxial layer.

* depth of difussion controlled, so that it does not penetrate thr n-layer into the substrate.

* This diffusion is utilized to form the base region - transistor, anode of diode & junction capacitor.
resistor



Step 6 : Emitter difussion



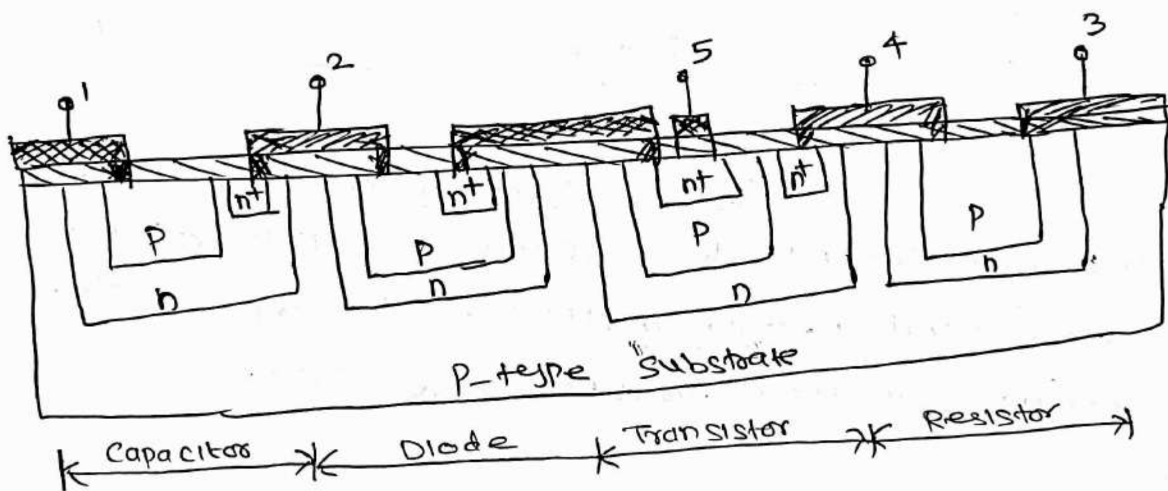
* New layer of SiO_2 is again grown over the entire wafer and Selectively etched to open a new set of windows and n-type impurities is diffused thru them. This forms transistor emitter and cathode region of diode
* windows are also etched into n-region where contact is to be made to the n-type layer.
* aluminium - used for making interconnection - P-type impurites in sillcon and produce unwanted rectifying contact with lightly doped n-material.

* Thus n^+ layer makes a good ohmic contact with Al-layer.

Step 7: Metallization

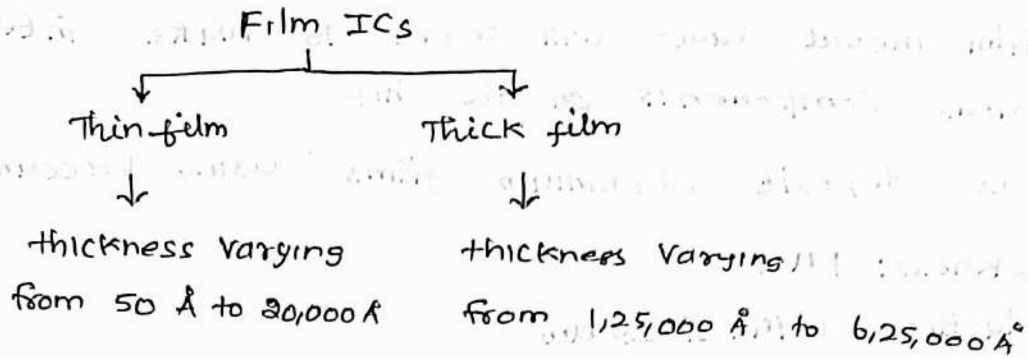
* IC is complete with all active and passive devices between the various components have to be made in accordance with the circuit.

* chip is further subjected to the process of formation of new SiO_2 layer and masked etching to open a new set of windows at the points where contacts have to be made.



* thin even coating of aluminium is vacuum deposited over the entire surface of the wafer. The interconnection pattern b/w the components is then formed by the photo resis technique.

Thick and thin film technology



* Film technology @ present can produce only passive components. mainly used for isolation or interconnections have to be made in ICs

* Thick film ICs are made by the process of screen printing. Thin film ICs are made by deposited on to substrates in a vaccum chamber

* Thick film ICs produce cheap and rugged resistors, capacitors and conducting patterns.

* Thin film technology provides greater precision in manufacturing but is more costly than thick film technology.

Deposition of Thin film

1. Vaccum evaporation
2. sputtering
3. Gas plating
4. Electroless plating
6. Silk screening

Vaccum Evaporation

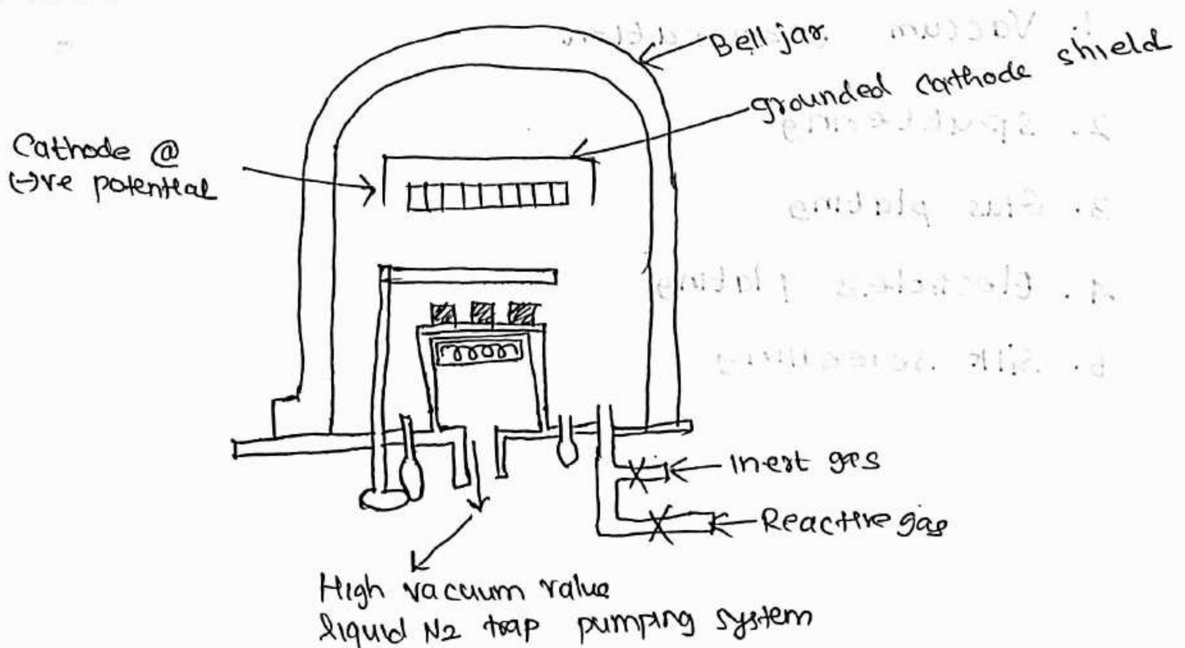
* thin film metal layer will serve to make interconnections of various components on the chip
* easy to deposit aluminium films using vaccum deposition

thickness: 1 μm
conduction width: 2-25 μm
pressure: 10^{-6} to 10^{-7} torr

"More points will be given in metallization"

Sputtering "Cathode Sputtering"

* almost identical to vaccum evaporation.
* performed @ low pressure (10^{-12} torr)
* much slower process
* source material: intense bombardment by the ions of a inert gas
* These gas ions are accelerated. potential: 2 to 5 kv
* potential applied between the cathode and anode, produces a glow discharge that fills the entire inter electrode space.



Plating Techniques

* Electroplating

Process of coating an object with one or more layers of different material/metals. Substrate & metal → immersed in an electrolytic solution. DC is passed thru it → ions migrated. This method suitable for making conductem films of gold or copper.

* Electroless plating

Metal ion solution is reduced to the free metal and deposited as a metallic coating without the use of electric current. This process can be used to deposit metals on any substrate such as glass, ceramic etc.,

Thick film Technology

(i) Screen printing (ii) ceramic printing

* process of screen printing ancient method. Screen used are woven from stainless steel wires to mesh size 320 and mounted on aluminium frame so as to keep the screen under uniform tension.

* Screen is next coated with a photo sensitive emulsion which polymerizes on exposure to light. A mask of desired pattern is made and kept on it.

* Screen becomes clear whereever thick film is to be deposited and blocked by photo resist.

* screen now placed on a substrate and carefully aligned components are deposited on the substrate thru screening process

* screening process carried out by a sequenced driven across the patterned screen at a constant rate.

* desired physical & electrical properties from thick film are deposited are now developed by thermal processing.

* it uses a furnace, where temperature varies from 500°c to 1000°c → called as firing process

* during firing, the organic binders of the thick film paste vaporises and the remaining material fuses with the substrate.

Surface mount technology

* advanced achievements in the area of semiconductor technology

* improve product size and technology (SMD) (surface mount devices)

* automation of manufacturing process as well as interconnection methodology can be achieved.

* SMT utilizes micro miniature leaded or leadless components called SMD

* Compact size of SMD → reduce the area in PCB → increase in packaging density.

* components & conductive path are installed on the same side of PCB.

Fabrication of Resistors

* Resistor - Monolithic IC - obtained by utilizing the bulk resistivity of the diffused volume of semi-conductor region. Commonly used methods

  (a) Diffused (b) Epitaxial (c) Pinched
  (d) thin film technique's.

Diffused Resistor

* formed in one of the isolated region of epitaxial layer during base or emitter diffusion.

* No extra fabricating steps required, so very economical resistor.

* Small range of resistances possible - limitation

* resistance value → determined by surface geometry such as length, width and the diffused impurity profile.

* Commonly used parameter - defining - Sheet Resistance R_s.

$$R = \rho \frac{L}{W \times t} \qquad R = R_s \frac{L}{W}$$

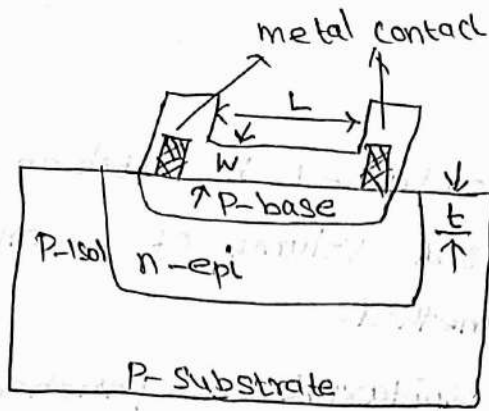
R → Resistance, ohm

R_s → Sheet resistance, ohms/square

L → length of diffused area

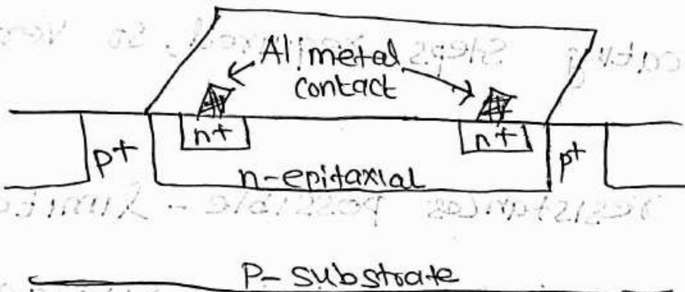
W → width of diffused area

* Base resistor - Range : 20 Ω to 300 kΩ - easily fabricated due to medium resistivity p type base region



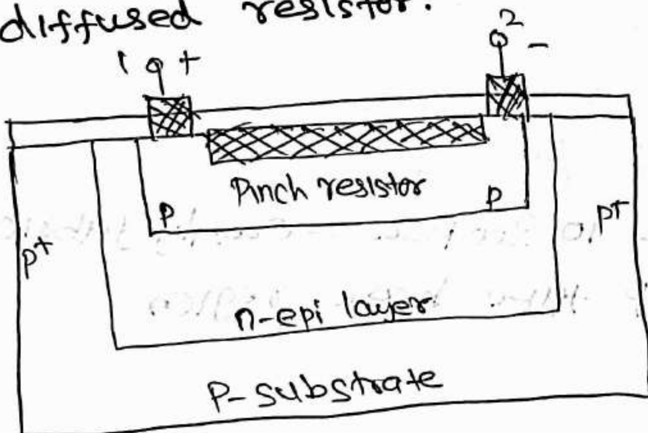
Epitaxial resistor

* N-epitaxial layer - used for - realizing large resistance values.
* R_S of epitaxial layer in the order of 1 to 10 k-Ω/square can be obtained.



Pinched resistor

* R_S of semiconductor region - increased - by reducing its cross sectional area.
* Used to achieve a high value of R_S from the ordinary base diffused resistor.



* Resistance of order mega ohm in smaller area
* No current flow through the n-type material due to diode at contact 2 in reverse direction
* only small reverse saturation current can flow thru n-type.

* Resistance b/w contact 1 & 2 increases as the width narrows down.

Thin film Resistors

* thin metallic film → Nichrome (NiCr) of thickness less than 1 μm is vapour deposited on the SiO_2 layer.

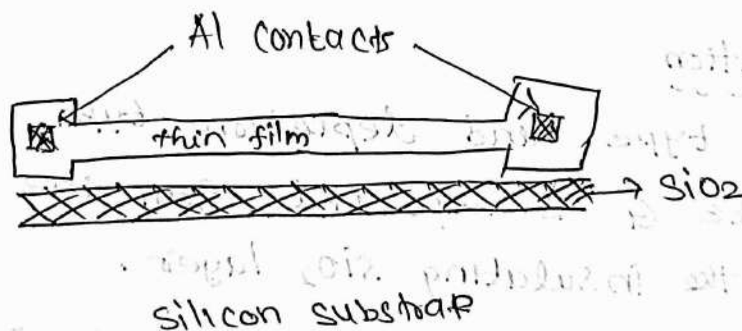
* thin film resistor can be obtained by the use of Tantalum deposited over silicon dioxide layer.

* Sheet Resistance 40 to 400 Ω/square
  resistance range : 20 kΩ to 50 kΩ

Advantage:

* have smaller parasitic components ; so high frequency behaviour is better
* Values are easily adjusted even after fabrication by laser trimming.
* have low temperature co-efficient; so more stable

Dis-advantage: Fabrication require additional process steps.



Fabrication of FET

* unipolar monolithic IC uses JFET or MOSFET as an active device

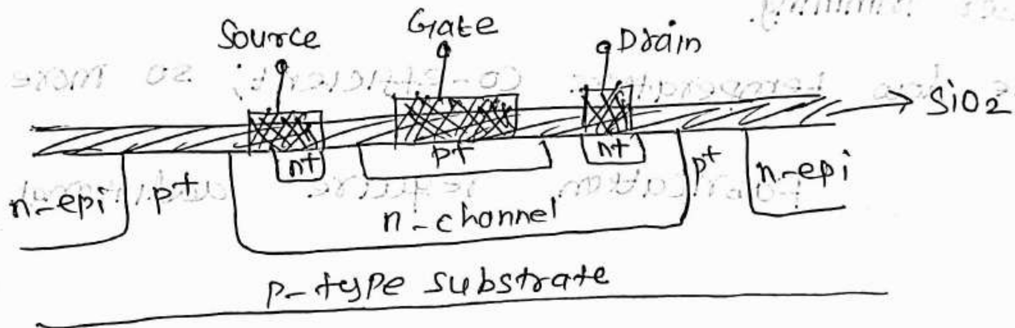
* FET → a device which flow of current thru the conducting region is controlled by an electric field.

JFET Fabrication

* Basic process similar to NPN or PNP BJT fabrication.
* epitaxial layer which formed the collector of the BJT is used as the n-chanel of the JFET.

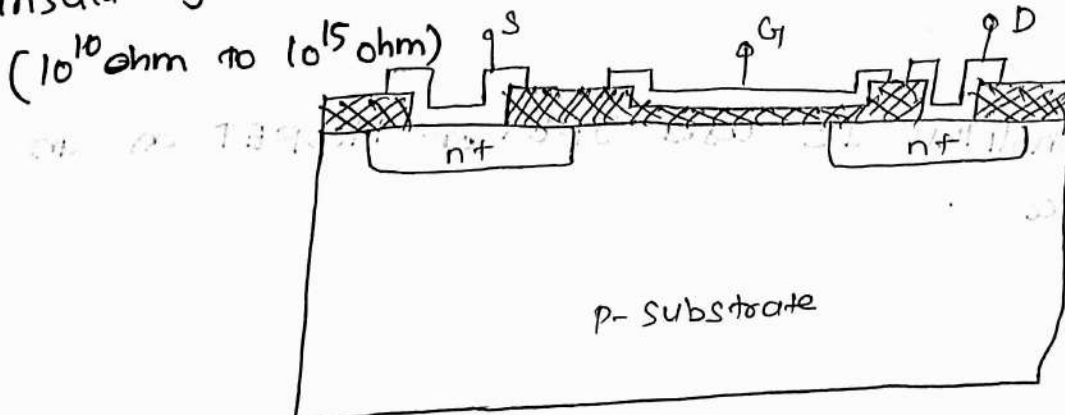
p^+ gate
↓
formed by diffusion or ion-implantation in n-channel

n^+ region
↓
formed by the drain and source contact regions to provide good ohmic contact.



JFET Fabrication

* Enhancement type and depletion type
* metallic gate G is seperated from the semiconductor channel by the insulating SiO_2 layer.
* insulating layer gives an extremely high input resistance. (10^{10} ohm to 10^{15} ohm)



V_T : 3 to 6 volt
$+V_{CC}$: 12 V

Use of Silicon Nitride (Si_3N_4)

* Si_3N_4 has superior masking property when compared to SiO_2

* Si_3N_4 sandwiched b/w two SiO_2 layer and provide the necessary barrier to prevent impurities penetrating through SiO_2 layer

$$\left.\begin{array}{l} Si_3N_4 \rightarrow 7.5 \\ SiO_2 \rightarrow 3.4 \end{array}\right] \text{Dielectric constant.}$$

* This increased overall dielectric constant redues V_T: threshold voltage.

Poly silicon gate

* when doped with phosphorus is conductive and used as gate electrode instead of aluminium.

* reduce V_T to about 1 to 2V. Such device are called silicon gate MOS transistor.

Si_3N_4: Coated to the entire surface of P-type wafer

Si_3N_4: Next to etched away from the surface outside the transistor region.

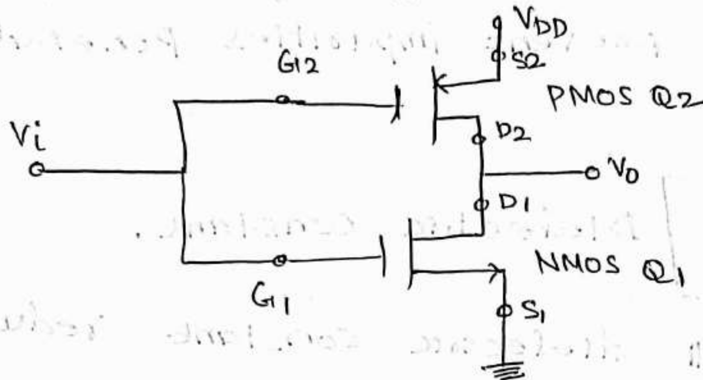
* two important points:

(a) No Isolation island is required.

(b) Facilitate self-alignment of the gate with the source and drain. This self-alignment property avoids any masking error and eliminates any additional capacitance.

CMOS Fabrication

* possible to fabricate NMOS and PMOS enhancement device on the same silicon chip.



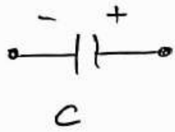
Fabrication of capacitor

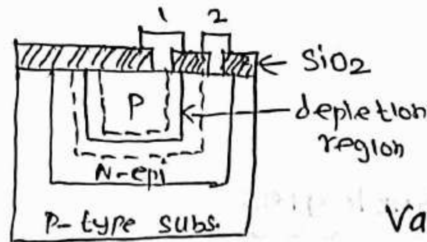
* Capacitor : two terminal passive device used to store potential energy in a electric field.
* consists of 2 parallel plate conductors seperated by a dielectric/insulator.

  * Junction capacitor
  * MOS and thin film capacitor

Junction Capacitor

* PN junctions have capacitance.
* p-region → one conducting plate
  N-region → other conducting plate
* depletion region between p and N forms dielectric.
* PN junction diode in reverse bias act as a capacitor.





$C \propto \frac{A}{T}$ → A → area of junction, T → depletion thickness

Value less than 100 pF

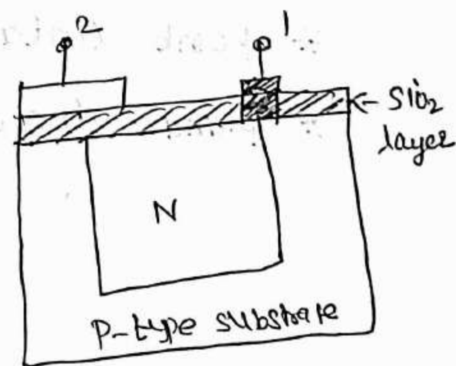
* P type substrate → generated by crystal growth technique.
* epitaxial layer of N-type silicon is grown over which oxidation takes place resulting in SiO_2 layer
* PN junction formation → photolithography diffusion
* metallization → contact mask

Mos and thin film capacitor

* Metal oxide silicon capacitor - parallel plate capacitor with SiO_2 as the dielectric.
* non polar capacitor (i.e.) no specified polarities.

Silicon Nitride → used as dielectric
offer high value of capacitance
higher dielectric constant

* heavily doped N-type epitaxial layer formed in p-type substrate. N-type layer forms the lower plate of capacitor. After epitaxial growth, oxidation takes place resulting in SiO_2 layer which act as dielectric. thin film of aluminium metallization forms the upper layer of capacitor



Fabrication of PV cell

(i) crystalline Si cell Technologies

* large semiconductor diode. 0.3mm thick taken from Si ingot

(ii) Amorphous Si cell Technologies → non-crystalline form of silicon

(iii) Thin film cell Technologies

Amorphous silicon (a-Si)
Cadmium telluride (CdTe)
Organic photovoltaic cells (OPC)
Copper Indium gallium selenide (CIS/CIGS)

Fabrication of PN junction diode

* Grown Junction diode
* Alloy type (or) fused junction diode
* Diffused Junction diode
* Point contact diode
* planar diffused diode

Comparison of npn and pnp Ic Transistor

* vertical pnp transistor has dis-advantage that its Collector has to be held @ a fixed (-)ve voltage

* lateral pnp transistor has inferior characteristics @ the base width is usally larger Controlled by lateral diffusion of p-type impurities and photographic limitations during mask making and alignment. ∴ pnp transistor gives current gain as low as 1.5 to 30 compared to 50 to 300 for the npn transistor. Now possible to increase gain as 100.

* The collector region is heated during Base & emitter diffusions. So the diffusion co-efficient of collector impurities should be as small as possible to avoid the movement of collector junction. Since n-type impurities have smaller diffusion constant than p-type impurities, the n-type [illegible] collector moves very little while p-type moves appreciably.

This makes npn transistor superior in performance with relatively easier process control.

CMOS Fabrication

* An n-type 'well' or 'tub' is diffused in p-type substrate. PMOS Transistor (Q_2) is fabricated

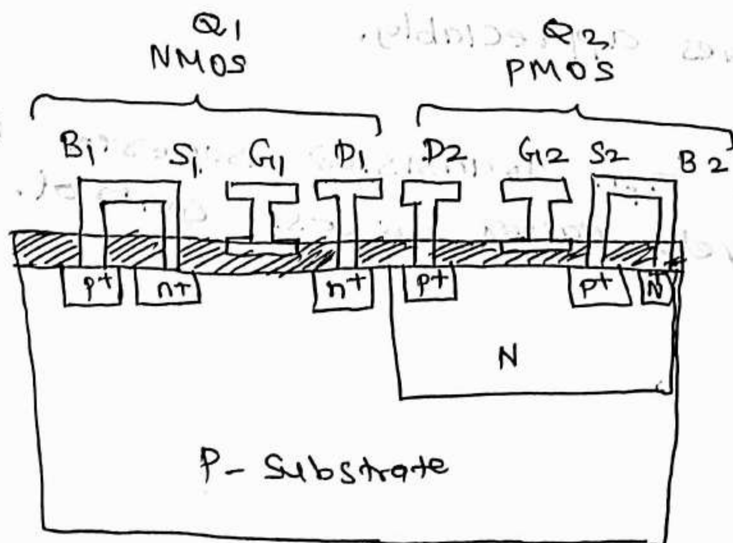
* n-type region : Body B_2 PMOS Transistor two additional steps required for PMOS Transistor Q_2 when compared to NMOS Transistor (Q_1).

* Two additional steps formation of n-region and ion implantation of p-type source and drain region

* B_1 tied to S_1 and connected to lowest voltage (GND) where B_2 tied to S_2 and held at supply voltage

* $B_1 \rightarrow$ p type ; $B_2 \rightarrow$ n type : $B_1 - S_1$, $B_2 - S_2$] diode reverse Bias cut off.

* Isolation b/w NMOS & PMOS automatically achieved



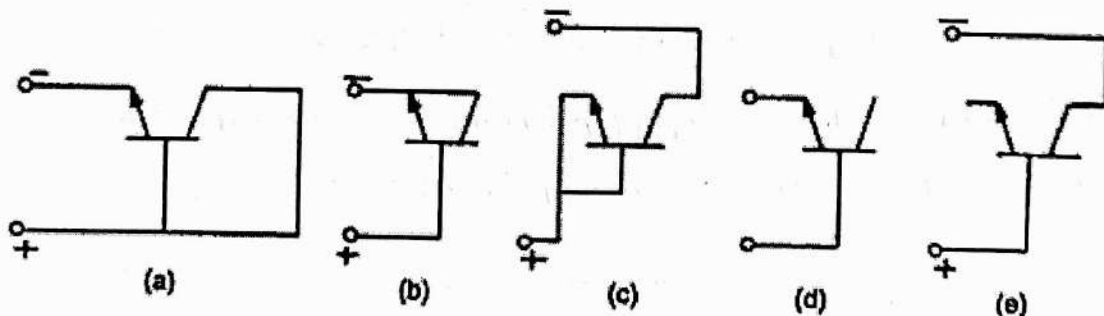
Monolithic diodes

The diode used in integrated circuits is made using transistor structures in one of the five possible connections. The three most popular structures are shown in figure. The diode is obtained from a transistor structure using one of the following structures.

1. The emitter-base diode, with collector short circuited to the base.
2. The emitter-base diode with the collector open and
3. The collector –base diode, with the emitter open-circuited.

The choice of the diode structure depends on the performance and application desired. Collector-base diodes have higher collector-base arrays breaking rating, and they are suitable for common-cathode diode arrays diffused within a single isolation island. The emitter-base diffusion is very popular for the fabrication of diodes, provided the reverse-voltage requirement of the circuit does not exceed the lower base-emitter breakdown voltage.

Characteristic	*(a)* $V_{CB} = 0$	*(b)* $V_{CE} = 0$	*(c)* $V_{EB} = 0$	*(d)* $I_C = 0$	*(e)* $I_E = 0$
Breakdown voltage in volts	7	7	55	7	55
Storage time, n sec	9	100	53	56	85
Forward voltage in volts	.85	.92	.94	.96	.95



* Diode '(a)' is most useful for getting high speed to be used in digital IC due to its lowest storage time and lowest forward voltage drop.

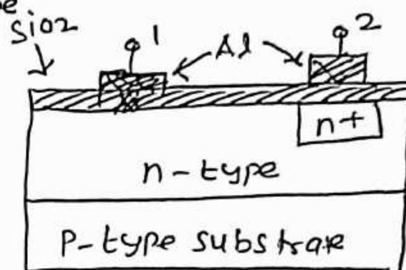
* Diode '(c)' and '(e)' → advantage of highest breakdown voltage

* Diode '(b)' and '(d)' → stored charge device → high speed turn off of the transistor.

Schottky Barrier Diode

* metal to semiconductor junctions can be ohmic as well as rectifying.
* ohmic contact is used when lead is to be attached to a semiconductor device and a rectifying contact called Metal semiconductor diode, (schottky Barrier diode), similar characteristics to an pn diode.

* Aluminium : p-type impurity in silicon. when it is used to make a contact with n-type silicon. This contact is ohmic and no pn junction is formed.



* This is done by making n+ diffusion in the n-regions near the surface where Al is deposited.
* physical mechanism is complicated and very different compared to p-n junction.
* Contact 1 : schottky barrier Contact 2 : ohmic contact
* contact potential b/w semiconductor & metal creates a barrier to the flow of conduction of electrons from SC → metal
* Forward biasing the junction lowers this barrier and permit flow of electron. Majority carrier carriers current in this diode
* Schottky diode exhibit negligible storage time (e^- from n-type Si enter Al @ the surface, where mix with free electrons)

Advantage: (i) less forward voltage (ii) used for ideal clamping ; detector in high frequency and microwave IC's.