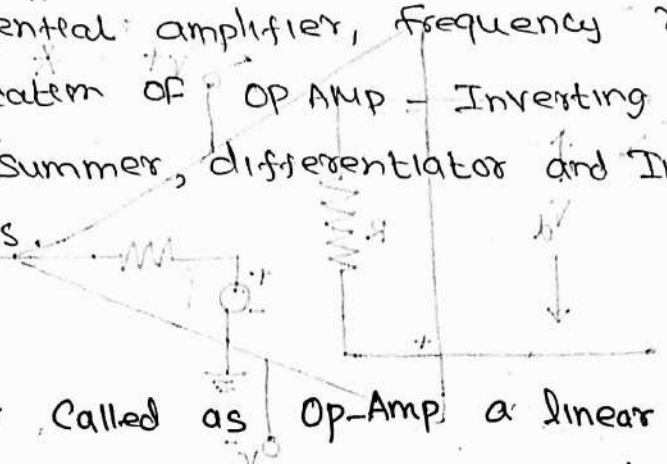
Unit-2

CHARACTERISTCS OF OP AMP

Ideal Op-Amp characteristics - DC characteristics, AC characteristics, differential amplifier, frequency response of Op-AMP, Basic applicatem of OP AMP - Inverting and Non-Inverting Amplifiers, Summer, differentiator and Integrator V/I and I/V converters.

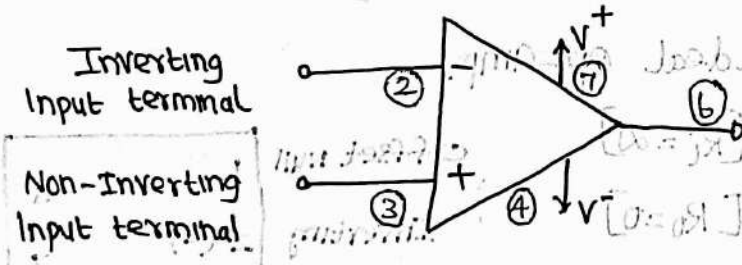


* Operational Amplifer called as Op-Amp a linear device.

Three stage circuit: Input stage, gain stage and output stage.

* Used extensively in signal conditioning, filtering or to perform mathemattcal operattons such as addition, subtracten, integratem, differentiation etc.,

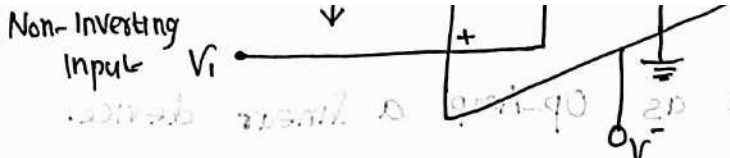
* Op-amp amplifies only the difference between two input signal and generates single output.



* Five Basic terminals - two input, One output and two power supply terminals.

Inverting amplifier: 180° phase difference blw Input-Output sgl

Non-Inverting amplifier: 0° phase difference blw Input-output sgl



If $V_1 = 0$, output V_0 is 180° out of phase with input sgl V_2.

If $V_2 = 0$, output V_0 will be in phase with input signal V_1

$$V_0 = A(V_1 - V_2)$$

Output in phase V_1

Output out of phase V_2

↳ inverting input terminal

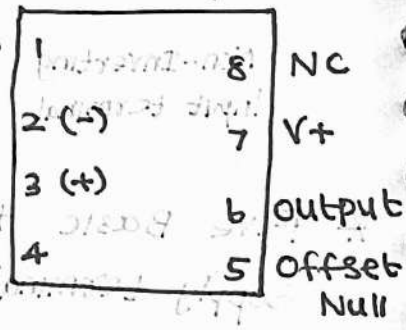
↓ non-inverting input terminal

↙ differential gain

$$V_0 = AV_d \quad [\because V_d = V_1 - V_2]$$

The characteristics of ideal op-amp:

* Infinite input resistance $[R_i = \infty]$
* Zero output resistance $[R_0 = 0]$
* Infinite Voltage gain $A_V = \infty$
* Infinite Band width $BW = \infty$
* Zero offset (i.e.,) when $V_1 = V_2$, $V_0 = 0$
* Slew Rate = infinite
* Common Mode Rejection Ratio CMRR $= \infty$

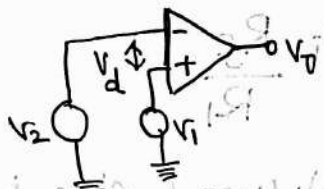


It can be observed that,

* draws no current at both input terminal [$i_1=0, i_2=0$]. Bcoz of infinite input Impedance, any sgl with source impedance can drive the op-amp w/o getting any loading effect.
* Gain is infinite. Hence, the voltage b/w the inverting & non-inverting terminal is essentially zero for an finite o/p voltage
* Output voltage V_0 is independent of the current drawn from the output $R_0=0$.

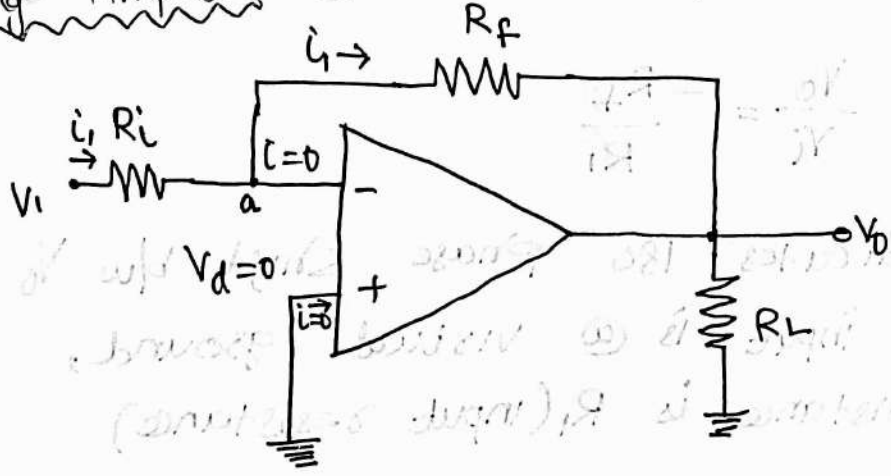
Open loop operation of Op-Amp

V_1 : Inverting
V_2 : Non-inverting



* Infinite gain, so V_0 is either at its +ve or -ve saturation region/voltage ($+V_{sat}/-V_{sat}$) as $V_1 > V_2$ or $V_2 > V_1$.
* Application: Voltage Comparator, Zero crossing detector.
* Amplifier acts as switch.

Inverting Amplifier



* output voltage (V_0) is fed back to the inverting input terminal through (R_f) feedback resistor.
* Input signal V_i applied to the inverting input terminal through R_1 and non-inverting input terminal - grounded.

Analysis: For simplicity, assume ideal op-amp
As $V_d = 0$,

$$i_1 = \frac{V_i}{R_1}$$

Also since op-amp draws no current, current thru R_1 must flow through R_f.

$$V_0 = -i_1 R_f = -V_i \frac{R_f}{R_1}$$

Gain of inverting amplifier (closed loop gain)

$$A_{CL} = \frac{V_0}{V_i} = -\frac{R_f}{R_1}$$

Alternatively, nodal equation @ node 'a',

$$\frac{V_a - V_i}{R_1} + \frac{V_a - V_0}{R_f} = 0 \qquad (V_a = 0 \text{ bcoz node a @ virtual ground})$$

$$\therefore A_{CL} = \frac{V_0}{V_i} = -\frac{R_f}{R_1}$$

* -ve sign indicates 180° phase shift b/w V_0 and V_i.
Also inverting input is @ virtual ground, effective Resistance is R_1 (input resistance)

* So, R_1 kept large to avoid loading effect.

$[R_f > R_1 \quad gain > 1]\ [R_f < R_1 \quad gain < 1]\ [R_f = R_1 \quad gain = 1]$

* load resistor R_L put at the output, otherwise the input importance of measuring device act as load.

* R_1 and R_f are replaced by Impedance then $A_{CL} = -\frac{Z_f}{Z_1}$

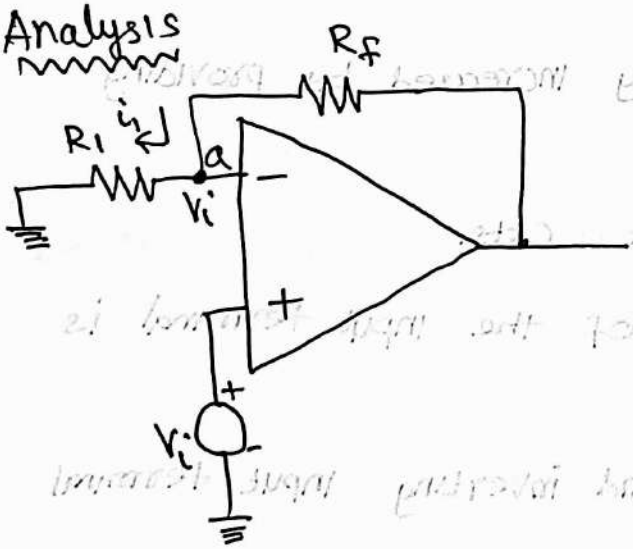
Non - Inverting Amplifier

* Amplifies the input without producing any phase shift between input and Output.

* Input signal – non inverting input terminal

* negative feedback sln output is fed back to the inverting input terminal.

Analysis



* V_d @ input terminal $= 0$

* nodal eqn @ node a

$$\frac{V_i - 0}{R_1} + \frac{V_i - V_0}{R_f} = 0$$

$$\frac{V_i}{R_i} = -\left(\frac{V_i - V_0}{R_f}\right)$$

$$\frac{V_i}{R_1} = -\frac{V_i}{R_f} + \frac{V_0}{R_f}$$

$$\frac{V_i}{R_1} + \frac{V_i}{R_f} = \frac{V_0}{R_f} \qquad V_i\left[\frac{1}{R_1} + \frac{1}{R_f}\right] = \frac{V_0}{R_f}$$

$$\frac{V_0}{V_i} = R_f\left[\frac{1}{R_1} + \frac{1}{R_f}\right]$$

$$= \frac{R_1 + R_f}{R_1}$$

$$A_{CL} = \frac{V_0}{V_i} = 1 + \frac{R_f}{R_1}$$

* Gain must be adjusted to unity by proper selection of resister R_f and R_1.
* Compared to inverting amplifier, R_i of non-inverting amplifier is extremely large ($=\infty$), op-amp draws negligible current from signal source.

Feedback in Ideal op-amp

* Utility of an op-amp can be greatly increased by providing negative feedback.
* two important negative feedback ckts.
  (a) current drawn by either of the input terminal is negligible
  (b) V_d between non-inverting and inverting input terminal is essentially zero.

1. Design an amplifier with a gain of −10 and input resistance equal to 10 kΩ

$R_1 = 10\ k\Omega$

$A_{CL} = -\frac{R_f}{R_1}$ $\qquad R_f = -A_{CL} \cdot R_1$

$= -(-10) \times 10\ k\Omega$

$= 100\ k\Omega$

2. A load of 25kΩ is connected to the output terminal. Calculate (i) i_1 (ii) V_0 (iii) i_L (iv) total current i_0 into the output pin. Consider $R_1 = 10\ k\Omega$ $R_f = 100\ k\Omega$ $V_i = 1V$

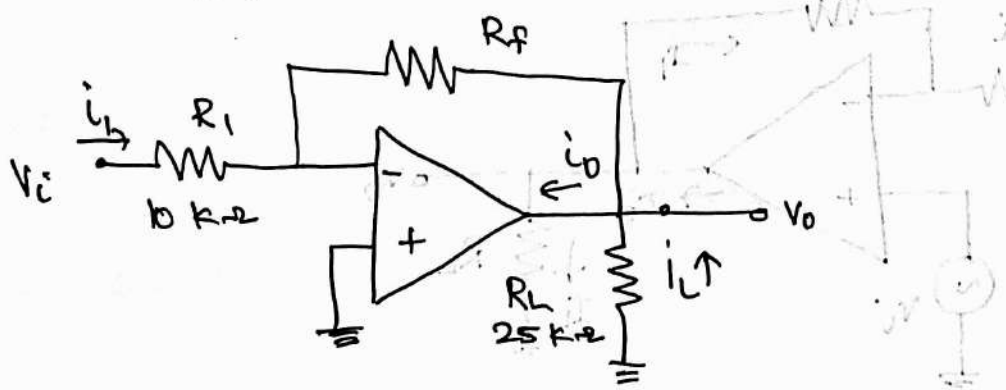
$$i_1 = \frac{V_i}{R_1} = \frac{1}{10\ k\Omega} = 0.1\ mA$$

$$\frac{V_0}{V_i} = -\frac{R_f}{R_1} \qquad V_0 = -\frac{R_f}{R_1} V_i$$

$$= -\frac{100\ k\Omega}{10\ k\Omega} 1V = -10V$$

$$i_L = \frac{V_0}{R_L} = \frac{10\ V}{25\ k\Omega} = 0.4\ mA$$

$$i_0 = i_1 + i_L = 0.1\ mA + 0.4\ mA = 0.5\ mA$$



Determine the voltage gain of an inverting amplifier with $R_1 = 10\ k\Omega$ $R_f = 47\ k\Omega$

$$A_{CL} = -\frac{R_f}{R_1} = \frac{-47 \times 10^3}{10 \times 10^3} = -4.7$$

$A_{CL} = 4.7$

negative sign indicates phase shift

A sine wave of 0.5V peak voltage is applied to an inverting amplifier using $R_1 = 10\ k\Omega$ $R_f = 50\ k\Omega$. It uses the supply voltage of ±12V. Determine the output voltage.

$R_1 = 10\ k\Omega$
$R_f = 50\ k\Omega$
$V_i = 0.5\ V$

$$A_{CL} = -\frac{R_f}{R_1} = \frac{-50k}{10k} = -5$$

$$A_{CL} = +\frac{V_0}{V_i} \qquad V_0 = V_i \cdot A_{CL}$$

$= 0.5 \times 5$

$= 2.5$ volt.

An input of 3V is fed to the non-inverting terminal of an op-Amp. The amplifier has $R_1 = 10\ k\Omega$ $R_f = 10\ k\Omega$. Find V_0.

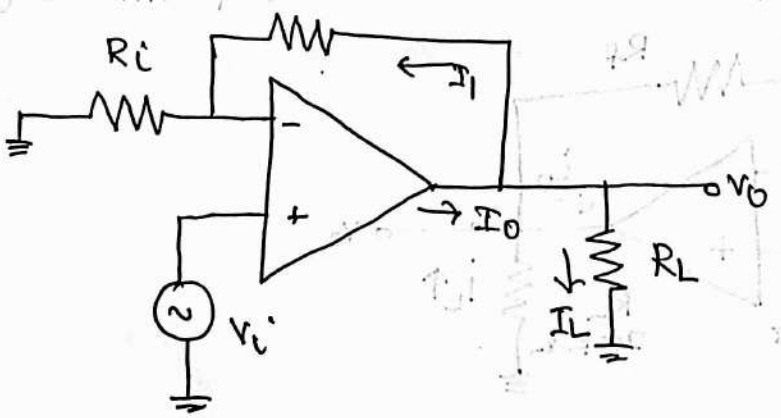
$V_i = 3V$ $R_1 = R_f = 10\ k\Omega$

$$A_{CL} = 1 + \frac{R_f}{R_1} = 1 + \frac{10}{10} = 2$$

$V_0 = V_i\ A_{CL}$

$= 3 \times 2 = 6$ Volt

For non-inverting amplifier, $R_1 = 5\ k\Omega$ $R_f = 20\ k\Omega$ $V_i = 1$ volt. $R_L = 5\ k\Omega$ connected at output. Determine V_0, A_{CL}, i_L and i_0



$$V_o = \left[1 + \frac{R_f}{R_1}\right] V_i = \left[1 + \frac{20\,k}{5\,k}\right][1V] = 5V$$

$$A_{CL} = \frac{V_o}{V_i} = \frac{5V}{1V} = 5$$

$$i_L = \frac{V_o}{R_L} = \frac{5V}{5k\Omega} = 1\,mA$$

$$i_1 = \frac{V_i}{R_1} = \frac{V_o - V_i}{R_f} = 0.2\,mA$$

$$i_o = i_1 + i_L = 0.2 + 1\,mA$$
$$= 1.2\,mA.$$

Design an amplifier with a gain of +5 using one op-amp

$$A_{CL} = 1 + \frac{R_f}{R_1}$$

$$5 = 1 + \frac{R_f}{10k} \qquad \frac{10k + R_f}{10k} = 5$$

$$R_f = 4 \times 10 = 40\,k\Omega$$

DC performance characteristics

* Ideal op-amp draws no current from source, response is also independent of temperature variations.
* real/practical op-amp shifts its operation with temperature.
* Due to mis-match of transistors, two inputs respond differently to input voltage and current.

These non-ideal dc characteristics that add error components to the dc output voltage are

* Input Bias current
* Input offset current
* Input offset voltage
* Thermal drift.

* Op amp input ↓ BJT/FET differential amplifier

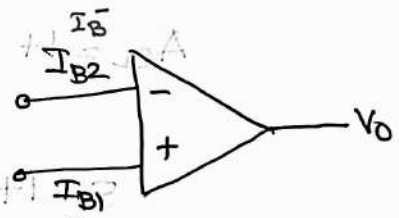
* Ideal op-amp : No current
* practical op-amp : current DC current

Input Bias current

* Input Bias current is the average of the current that flows into the inverting and non-inverting input terminals of an op-amp.

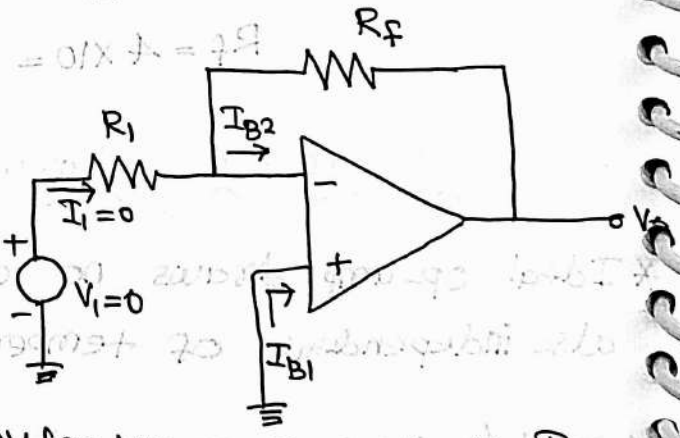
* this current affects all the application of op-amp.
* pratically, input terminals do conduct a small value of dc current to bias the input transistor.

FET : pA BJT : μA IC741 = 80nA



* when lower input bias currents are achieved the possible imbalances in the circuit will be minimized.

I_{B1} and I_{B2} : Base current



* though transistor are identical $I_{B1} \neq I_{B2}$ due to imbalances during fabrication. Hence manufacturers specify the I_B.

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

I_{B1} : Bias current entering non-inverting input

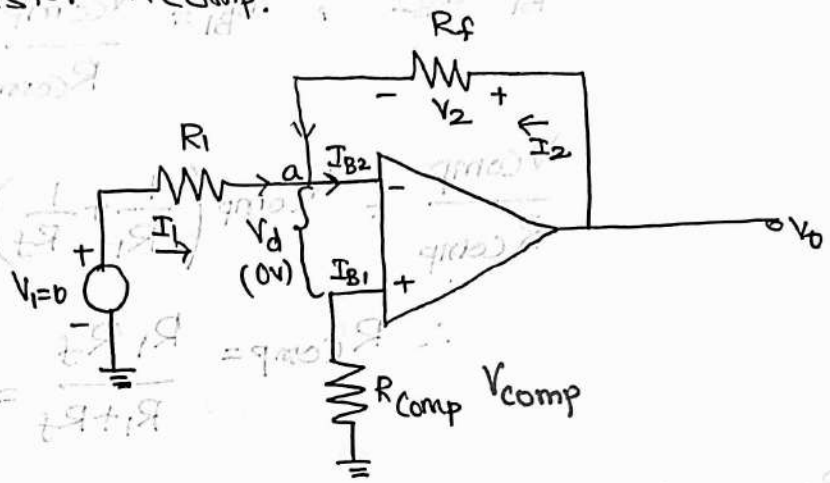
I_{B2} : Bias current entering inverting input

Consider the basic inverting amplifier, If $V_i = 0$ then $V_0 = 0$
However V_0 is found to be offset by a value of

$$V_0 = (I_{B2})R_f$$

Application sgl level & measured in millivolt, is not acceptable.

This offset effect can be compensated by the use of a Compensation Resistor R_{comp}.



The current I_{B1} flowing thru R_{comp} develops a voltage V_{comp} across it.

Apply KVL,

$$-V_{comp} + 0 + V_2 - V_0 = 0$$

$$V_0 = V_2 - V_{comp}$$

So to achieve $V_0 = 0$ proper R_{comp} should be selected to get $V_2 = V_{comp}$ and thus offset effect gets cancelled.

To find R_{comp}:

$$V_{comp} = R_{comp} I_{B1} \quad \therefore R_{comp} = \frac{V_{comp}}{I_{B1}}$$

KCL at node a, $I_{B2} = I_1 + I_2$

Entering current @ node = leaving current @ node

$$I_1 = \frac{V_{comp}}{R_1} \qquad I_2 = \frac{V_2}{R_f}$$

For offset compensation $V_2 = V_{comp}$

$$I_2 = \frac{V_{comp}}{R_f}$$

$$\therefore I_{B2} = \frac{V_{comp}}{R_1} + \frac{V_{comp}}{R_f}$$

$$I_{B2} = \left(\frac{1}{R_1} + \frac{1}{R_f}\right) V_{comp}$$

Assume $I_{B1} = I_{B2}$, $I_{B1} = \frac{V_{comp}}{R_{comp}}$

$$\frac{V_{comp}}{R_{comp}} = V_{comp}\left(\frac{1}{R_1} + \frac{1}{R_f}\right)$$

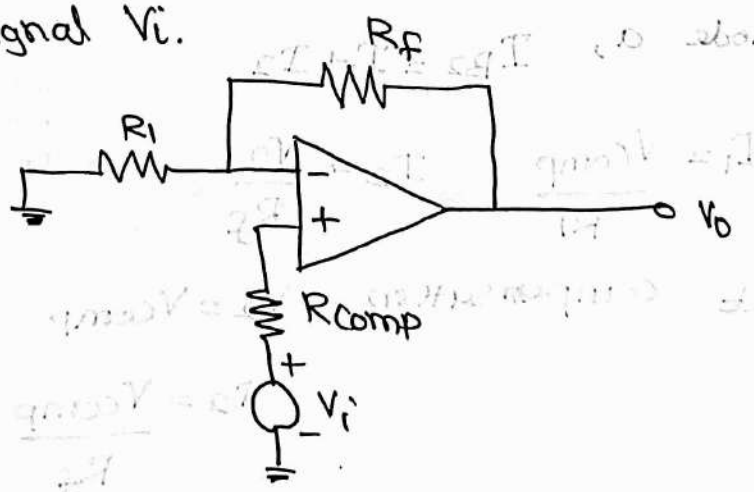
$$\therefore R_{comp} = \frac{R_1 R_f}{R_1 + R_f} = R_1 \parallel R_f$$

R_{comp} must be equal to the parallel combination of input and feedback resistors connecting @ the inverting input terminal

For non-inverting amplifier,

$$R_{comp} = R_1 \parallel R_f$$

effect of I_B compensated by R_{comp} in series with input signal V_i.



Input offset current

* I_B compensation is achieved when I_B are equal $I_{B1} = I_{B2}$
* But input transistor cannot be made identical and there exists diff. b/w I_{B1} and I_{B2}. The difference in magnitude b/w I_{B1} and I_{B2} → input offset current I_{OS}

$$I_{OS} = |I_{B1}| - (I_{B2})$$

To find the effect of I_{OS} consider the bias current compensation circuit assuming $V_i = 0$

$$V_o = V_2 - V_{comp}$$

$$V_o = I_2 R_f - V_{comp}$$

$$I_{B2} = I_1 + I_2$$

$$I_2 = I_{B2} - I_1$$

$$I_2 = I_{B2} - \frac{V_{comp}}{R_1} \quad \left[I_1 = \frac{V_{comp}}{R_1}\right] \quad \left[V_{comp} = I_{B1} \cdot R_{comp}\right]$$

$$I_2 = I_{B2} - I_{B1} \frac{R_{comp}}{R_1}$$

$$\left(V_{comp} = I_{B1} \cdot R_{comp}\right)$$

$$\therefore V_o = \left(I_{B2} - I_{B1} \frac{R_{comp}}{R_1}\right) R_f - I_{B1} \cdot R_{comp}$$

$$= I_{B2} R_f - \frac{I_{B1} R_f R_{comp}}{R_1} - I_{B1} R_{comp}$$

$$= \left[I_{B2} - \frac{I_{B1} R_{comp}}{R_1}\right] R_f - I_{B1} R_{comp}$$

use $R_{comp} = \frac{R_1 R_f}{R_1 + R_f}$ in above eqn we get

* BJT 200 nA
  FET 10 pA
* magnitude sign → no way to predict which of the bias currents will be larger

$$\boxed{V_o = R_f (I_{B2} - I_{B1})}$$

$$\boxed{V_o = R_f \, I_{os}}$$

$$V_o = \left[I_{B2} - \frac{I_{B1}(R_1 R_f)}{R_1(R_1+R_f)} \right] R_f - \frac{I_{B1} R_1 R_f}{R_1+R_f}$$

$$= \left[\frac{I_{B2} R_1(R_1+R_f) - I_{B1} R_1 R_f}{R_1(R_1+R_f)} \right] R_f - \frac{I_{B1} R_1 R_f}{R_1+R_f}$$

$$= \frac{I_{B2} R_1 R_f(R_1+R_f) - I_{B1} R_1 R_f^2}{R_1(R_1+R_f)} - \frac{I_{B1} R_1 R_f}{R_1+R_f}$$

$$= \frac{I_{B2} R_1 R_f (R_1+R_f) - I_{B1} R_1 R_f^2 - I_{B1} R_1 R_f}{R_1+R_f}$$

$$= \frac{I_{B2} R_f R_1 + I_{B2} R_f^2 - I_{B1} R_f^2 - I_{B1} R_1 R_f}{R_1+R_f}$$

$$= \frac{I_{B2} R_f (R_1+R_f) - I_{B1} R_f (R_f - R_1)}{R_1+R_f}$$

$$= \frac{I_{B2} R_f (R_1+R_f) + I_{B1} R_f (R_1+R_f)}{R_1+R_f}$$

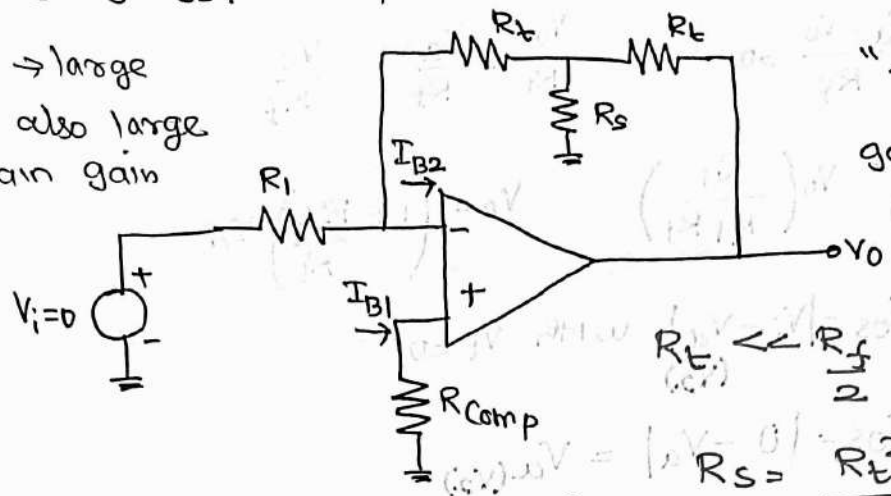
$$= I_{B2} R_f \oplus I_{B1} R_f = R_f (I_{B2} - I_{B1})$$

$$\boxed{V_o = R_f \, I_{os}}$$

Offset current can be minimized by keeping $R_f \rightarrow$ small

R_f value has to be large to compensate the effect produced by I_{os}. Compensatem of I_{os}

If $R_1 \rightarrow$ large
R_t also large
To obtain gain



"T-network is a good solution"

$R_t << \frac{R_f}{2}$ (To design a 'T' network)

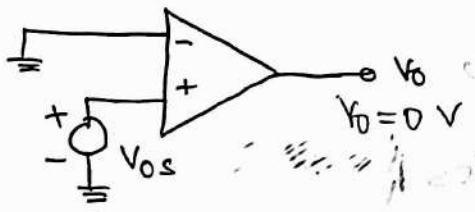
$$R_s = \frac{R_t^2}{R_f - 2R_t}$$

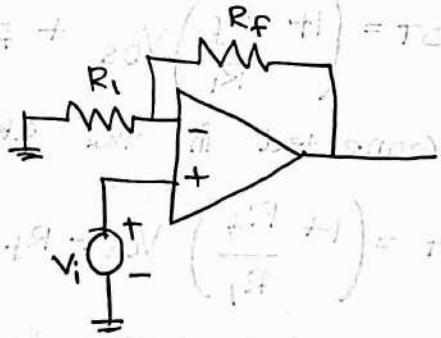
$$R_f = \frac{R_t^2 + 2R_tR_s}{R_s}$$

Input offset Voltage

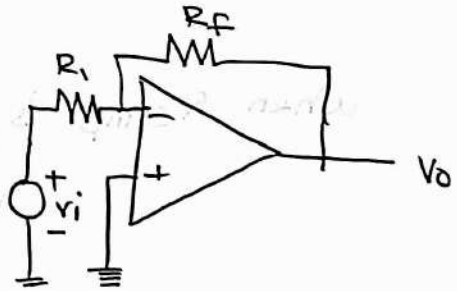
* defined as Voltage that is to be applied b/w two input terminals for making the output voltage zero.

* I/p offset Voltage – introduced due to mismatches in the O/p transistor and active load resistor.
Unavoidable imbalances

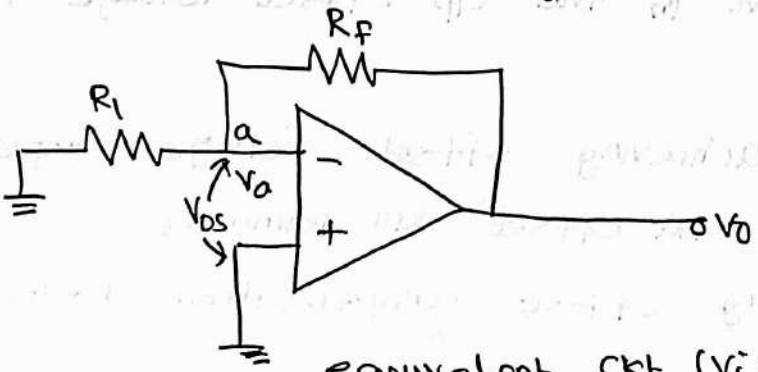




Non-Inverting



Inverting



equivalent ckt ($V_i = 0$)

Nodal equation @ node a

$$\frac{V_a - 0}{R_1} + \frac{V_a - V_o}{R_f} = 0 \qquad \frac{V_a}{R_1} + \frac{V_a}{R_f} = \frac{V_o}{R_f}$$

$$V_a = V_o\left(\frac{R_1}{R_1 + R_f}\right) \qquad V_o = \left(1 + \frac{R_f}{R_1}\right) V_a$$

V_a/V_2

V_a (V_2)

$$V_{os} = |V_i - V_a| \text{ with } V_i = 0$$

(V_2)

$$V_{os} = |0 - V_a| = V_{a(V_2)}$$

$$V_{os} = \left(1 + \frac{R_f}{R_1}\right) V_{os}$$ Output offset voltage in closed loop configuration.

Total output offset voltage

* V_{OT} can be due to either the I_B or the V_{os} and also it can be either +ve or −ve wrt ground. Considering both effects the total output offset voltage is

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{os} + R_f I_B$$

When R_{comp} is connected in the ckt,

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{os} + R_f I_{os}$$

Since $I_{os} < I_B$, it can be seen that the use of R_{comp} ensures a reduction in the o/p offset voltage generated due to I_B.

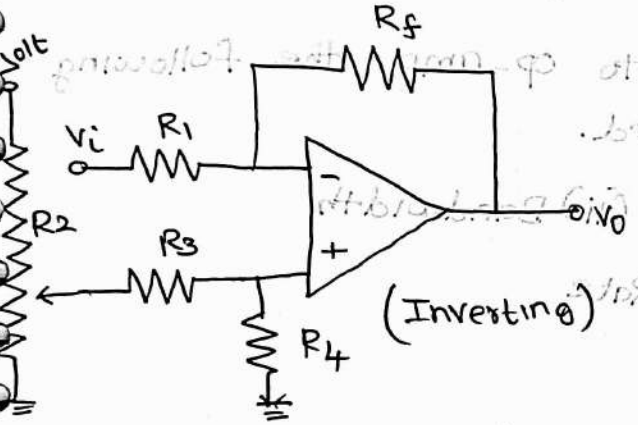
Two methods of achieving offset voltage compensation.

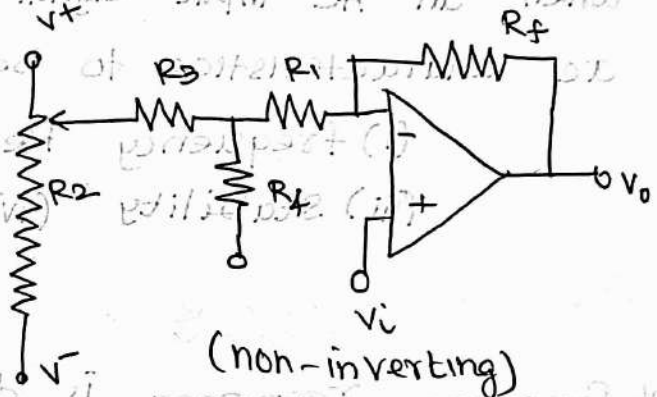
* op-amp with offset null terminals
* connecting offset compensation network.

* In op-amp with offset null terminal method manufacturer recommend a 10 kΩ potentiometer to be placed across offset null pin 1 and 5 and the wiper to be connected to the negative supply pin 4.

* when no offset null pins are provided external balancing techniques are used.

$$V_{OS} = \pm V \left(\frac{R_3}{R_3 + R_4} \right) \qquad A_V = \frac{V_O}{V_i} = 1 + \frac{R_f}{R_1 + R_f}$$





Thermal drift

* I_B, I_{OS}, V_{OS} → changes with temperature
* Change in temperature ΔT, change in time Δt, change in supply voltage ΔV_i will create a challenge to those parameter.
* ΔT cause most serious variation in the value of I_B, I_{OS}, V_{OS}.
* Thermal drift → used to identify such changes and defined as average rate of change of input offset voltage per unit change in temperature.

$\frac{\Delta V_{os}}{\Delta V_T}$ Unit: $\mu V/^\circ C$

Thermal drift → input offset current $\frac{\Delta I_{os}}{\Delta T}$ (pA/°C)

→ input bias current $\frac{\Delta I_B}{\Delta T}$ (pA/°C)

Thermal drift ⟶ not a constant value

→ not uniform over a specified Temperature range

AC performance characteristics

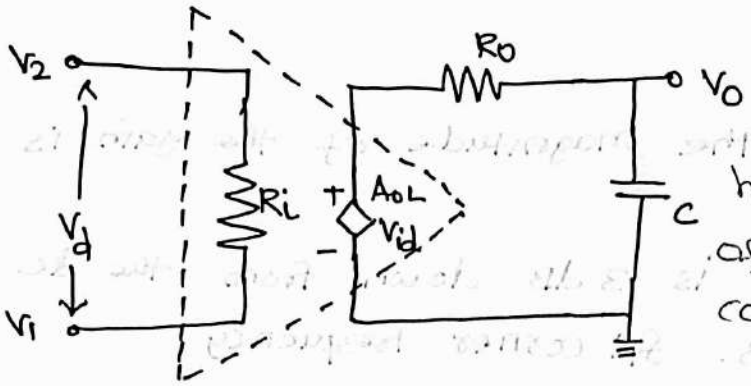
When an AC input signal applied to op-amp the following ac characteristics to be studied.

(i) frequency Response (ii) Bandwidth

(iii) Stability (iv) Slew Rate

Frequency Response

* frequency response is defined as the manner in which the gain of op-amp responds to different frequencies.
* Ideal op-amp has infinite bandwidth. ie) if its open loop gain is 90dB with dc signal its gain remains the same 90 dB through audio and onto high frequencies.
* Gain of practical op-amp decreases @ high frequencies. bcoz of capacitive component in the equivalent ckt of op-amp
* Capacitive component → present due to the stray capacitances or physical characteristic of device.



high frequency model of an op-amp with single corner frequency

Open loop voltage gain of an op-amp with only one corner frequency is obtained from

$$V_o = \frac{-jX_c}{R_o - jX_c} A_{OL} V_d$$

$$A = \frac{V_o}{V_d} = \frac{A_{OL}}{1 + j2\pi f R_o C} = \frac{A_{OL}}{1 + j(f/f_1)}$$

$$f_1 = \frac{1}{2\pi R_o C}$$

A_{OL} = Open loop gain @ low frequency

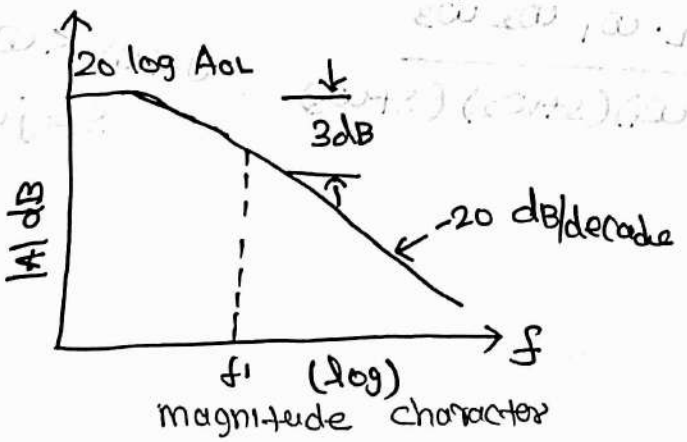
f_1 = break frequency / dominant pole frequency

The magnitude

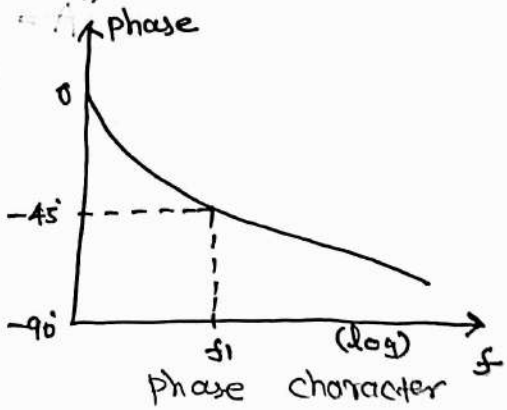
$$|A| = \frac{A_{OL}}{\sqrt{1 + (f/f_1)^2}}$$

The phase angle

$$\phi(f) = -\tan^{-1}(f/f_1)$$



magnitude character



phase character

From magnitude curve,

* Frequency $f << f_1$, the magnitude of the gain is $20 \log A_0$ in dB
* At $f = f_1$, the gain is 3 dB down from the dc voltage/ Value of A_0 is dB. f_1: corner frequency
* $f >> f_1$, the gain rolls off at the rate of -20 dB/decade

From phase plot,

* At $f = 0$, phase angle is Zero
* At f_1, phase angle is -45° lagging
* At infinite phase angle is -90°. this shows the maximum of phase shift, 90° can occur with a single capacitor.

The Voltage transfer function in s-domain

$$A = \frac{A_{OL}}{1 + j\left(f/f_1\right)} = \frac{A_{OL}}{1 + j\left(\frac{\omega}{\omega_1}\right)} = \frac{A_{OL}\,\omega_1}{j\omega + \omega_1} = \frac{A_{OL}\,\omega_1}{s + \omega_1}$$

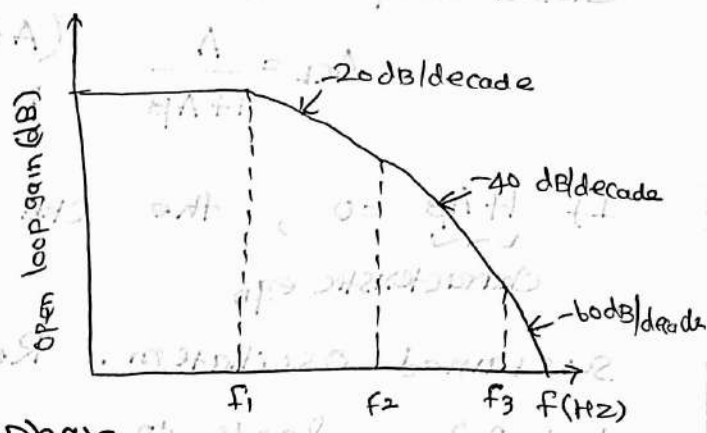
A practical op-amp has number of stages and each stage produce a different capacitive component. The transfer function with three break frequency

$$A = \frac{A_{OL}}{(1 + jf/f_1)(1 + jf/f_2)(1 + jf/f_3)} \qquad 0 < f_1 < f_2 < f_3$$

$$A = \frac{A_{OL} \cdot \omega_1 \omega_2 \omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)} \qquad 0 < \omega_1 < \omega_2 < \omega_2$$

$$s = j\omega$$

As frequency increases, cascading effect of RC pair (Poles) come into effect. Roll off rate increased by -20dB/decade @ each corner frequency.



Each pole also introduce lagging phase of maximum upto -90°

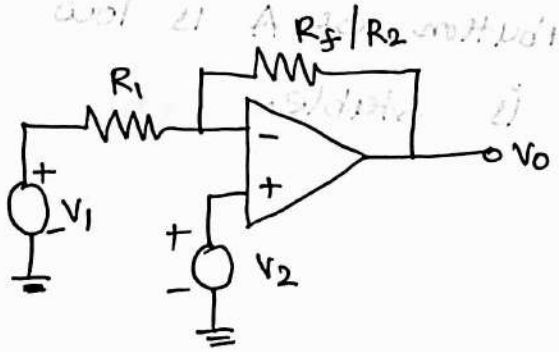
Bandwidth with feedback

* Bandwidth of an amplifier - range of frequencies within which the gain remain constant
* gain and Bandwidth → inversely proportional to one another
* gain x Bandwidth → always constant
* Bandwidth → increased → providing feedback sgl to input

$$\boxed{A_{CL}\, BW_{CL} = A_{OL}\, B_{OL}}$$

Stability of an op-amp

* op-amp rarely used in open loop configuration bcoz of high gain
* Let us consider Resistive feedback inverting amplifier ($V_2 = 0$)



closed loop t.f.n

$$A_{CL} = \frac{A}{1+A\beta}$$

(A = open loop voltage gain
β = feedback ratio)

If $\underbrace{1+A\beta}_{\text{characteristic eqn}} = 0$, the ckt becomes unstable; it leads to sustained oscillatem. Rewrite the characteristic eqn $1-(-A\beta)=0$ leads to

loop gain $-A\beta = 1$, which is complex quantity

So, magnitude $|A\beta| = 1$

phase condition

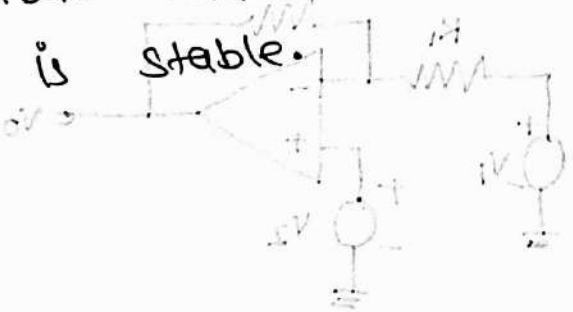
$$\angle A\beta = 0 \text{ (or multiple of } 2\pi)$$

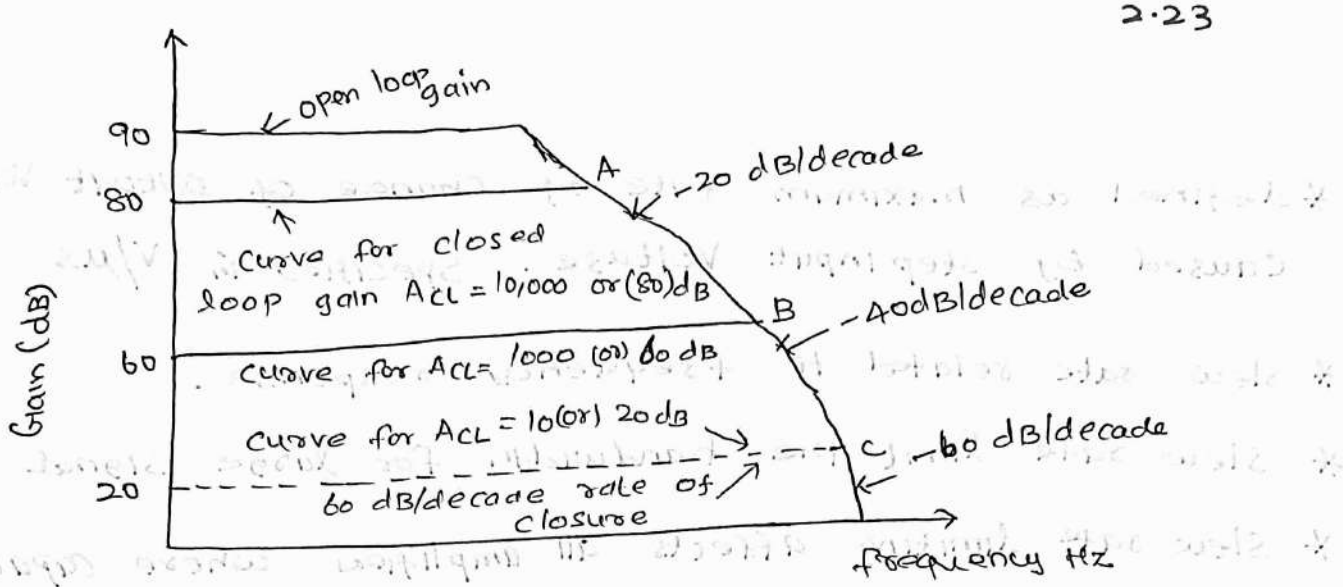
$$\angle A\beta = \pi \text{ (or odd multiple of } \pi)$$

Here β is a constant if only resistive components are used and hence they do not provide any phase shift.

When $(1+A\beta) < 1$, $A\beta < 0$ (i.e) $A\beta$ = negative value, which results in instability or unbounded output. Then $A_{CL} > A$, (i.e) closed loop gain increases and leads to stability.

In a given resistive feedback n/w, there is no phase shift. Since op-amp is connected in inverting mode, it provide a phase shift of 180° @ low frequencies. and contribution of A is low so $A\beta > 0$ $A_{CL} < A$ and the s/m is stable.





* At high frequency, at each corner frequency an additional phase shift of $-90°$ takes place. For two corner frequency additional phase shift will be $-180°$.

* @ high frequency, for some value of β, the magnitude of $A\beta$ become unity and an additional phase shift of $180°$ makes phase shift to zero. leads to amplifier to oscillate and unstable.

* From graph, three break pts → leads to $-270°$ phase shift resulting in unstable operation.

* For stable operation, the rate of closure b/w A_{CL} and A_{OL} curve should not exceed -20dB/decade.

transfer function with three poles,

$$A = \frac{A_{OL}\,\omega_1\omega_2\omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)} \qquad 0 < \omega_1 < \omega_2 < \omega_3$$

$1 + A\beta = 0$

$\therefore$ The poles $\quad 1 + \dfrac{\beta A_{OL}\,\omega_1\omega_2\omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)} = 0$

Slew Rate

* defined as maximum rate of change of output voltage caused by step input voltage. Specified in V/μs
* Slew rate related to frequency response.
* Slew rate limit the bandwidth for large signal output
* Slew rate limiting affects all amplifiers where capacitance has to be charged and discharged as voltage level vary.

Causes of Slew Rate

* Slew rate caused due to limited charging rate of the compensating capacitor, current limiting and saturation of the internal stages of an op-amp.

The rate @ which voltage across capacitor

$$\frac{dV_c}{dt} = \frac{I}{C}$$ (I = maxi. current furnished by op-amp to capacitor C)

Op-amp must have either a higher current or a small compensation capacitor. Slew rate reduces due to rise in temperature.

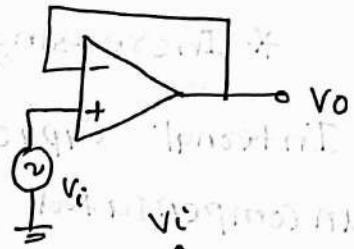
IC 741, $I_c = 15\ \mu A$ $C = 30\ pF$

$$\text{Slew rate} = \frac{dV_c}{dt} = \frac{I_{max}}{C}$$

$$= \frac{15\ \mu A}{30\ pF} = 0.5\ V/\mu s$$

Slew Rate limiting of sine wave

* S.R limits the response of all the large signal wave-shapes

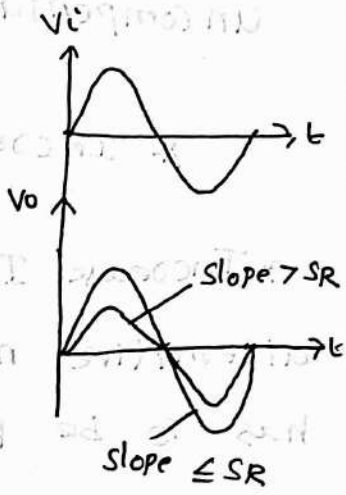


$V_i = V_m \sin \omega t$

$V_o = V_m \sin \omega t$

Rate of change of o/p,

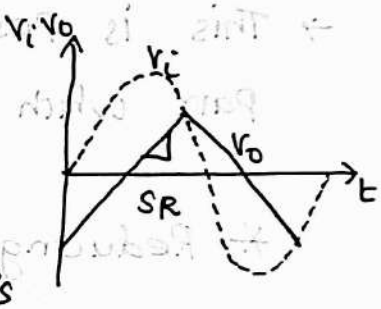
$$\frac{dV_o}{dt} = V_m \omega \cos \omega t$$



Maximum rate of change of o/p occur when $\cos \omega t = 1$

$$SR = \left.\frac{dV_o}{dt}\right|_{maxi} = V_m \omega \qquad (\omega = 2\pi f)$$

$$SR = 2\pi f V_m \ V/s = \frac{2\pi f V_m}{10^6} \ V/\mu s$$



$$f_{max} = \frac{SR}{2\pi V_m} \qquad V_{m(max)} = \frac{\text{Slew Rate}}{2\pi f}$$

↓ full power response

↓ maximum peak (max frequency of a sinusoidal voltage large amplitude sine wave which op-amp have w/o distortion)

$$FPB = \frac{SR}{2\pi V_{sat}}$$

↙ Full power Bandwidth

$\pm V_{sat}$ = Saturation Voltage

maximum frequency at which op-amp can produce an undistorted o/p with maximum possible amplitude.

Methods of improving Slew Rate

* Increasing f_1 (gain bandwidth product)

Internal capacitor value must be reduced. For uncompensated op-amps, compensating n/w be used

* Increasing $I_{01(sat)}$ (saturation current level of input stage)

→ Increase I_{01} w/o affecting the value of g_{m1} and f_t an alternative method for charging and discharging of C has to be provided.

→ This is possible by using additional input transistor pair which will go into conduction region.

* Reducing g_{m1}

→ g_{m1} can be reduced by using suitable resistance in series with the emitter of differential input transistors.

→ use FET instead of BJT differential input pair

* By using proper frequency compensation and other compensating networks higher slew rate op-amps can be selected for high speed applications.

Assuming slew rate for 741 is 0.5 V/μs. what is the maximum undistorted sine wave that can be obtained for 12V and 2V peak?

$$f_{max} = \frac{S.R}{2\pi V_m} = \frac{0.5\ V/\mu s}{2\pi \times V_m}$$

if $V_m = 12V$ then $f_{max} = 6.63\ KHz$

if $V_m = 2V$ then $f_{max} = 39.8\ KHz$

IC 741 is used as an inverting amplifier with a gain of 100. The voltage gain Vs frequency curve is flat up to 10 kHz. Determine the maximum peak to peak input signal that can be applied without any distortion to the output

$$V_{m(max)} = \frac{\text{Slew Rate}}{2\pi f}$$

$$= \frac{0.5\ V/\mu s}{2\pi \times 10\ KHz} = \frac{0.5}{2\pi \times 10 \times 10^3 \times 10^{-6}} = 7.96\ \text{Volt}$$

The output voltage of a certain op-amp circuit changes by 20 volt in 4μs. what is slew rate?

$$\text{Slew Rate} = \frac{dV_o}{dt}$$

$$= \frac{20\ V}{4\mu s} = 5\ V/\mu s$$

Frequency Compensation

* Achieve large Bandwidth and lower closed loop gain Suitable compensation techniques used

  (a) External Compensation

  (b) Internal Compensation

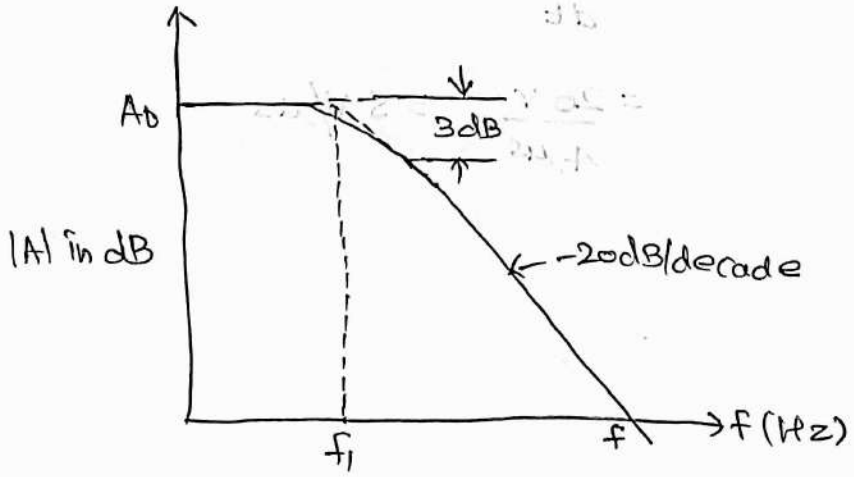
Internal frequency Compensation

* Broad Bandwidth may not be required for some applications. Such cases internally compensated op-amps called compensated op-amp can be employed

* found to be stable - regardless of value of closed loop gain and w/o any external compensation methods

* Op-amp 741 internally contains a capacitance of 30 pF that shunts off the sgl current @ higher frequencies, leading to decrease in O/p sgl

* Internal compensation capacitor causes the open loop gain to roll off @ -20dB/decade that assure a stable characteristic for the ckt.



External frequency compensation

* Compensating n/w connected externally to the op-amp for modifying the response suiting the requirement.
* −20 dB/decades – roll off rate – achieved by compensating n/w
* Commonly used external compensation:
  (a) Dominant pole compensation
  (b) Pole-zero (lag) compensation
  (c) Miller effect compensation

Dominant pole compensation

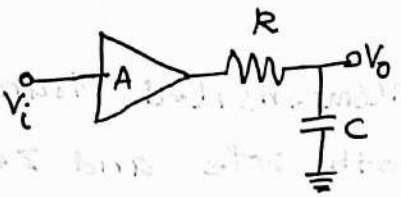
Assume A → uncompensated transfer function,

$$A = \frac{A_0 \omega_1 \omega_2 \omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)} \qquad 0 < \omega_1 < \omega_2 < \omega_3$$

For compensation introduce a dominant pole by adding RC-network in series with op-amp or by connecting a capacitor C from a suitable high resistance point to ground.

$$A' = \frac{V_0}{V_i} = A \cdot \left[\frac{1/j\omega C}{R + 1/j\omega C}\right]$$

$$= \frac{A}{1 + j(f/f_d)}$$



Dominant pole compensation

$f_d = \frac{1}{2\pi RC}$, break frequency of compensating n/w.

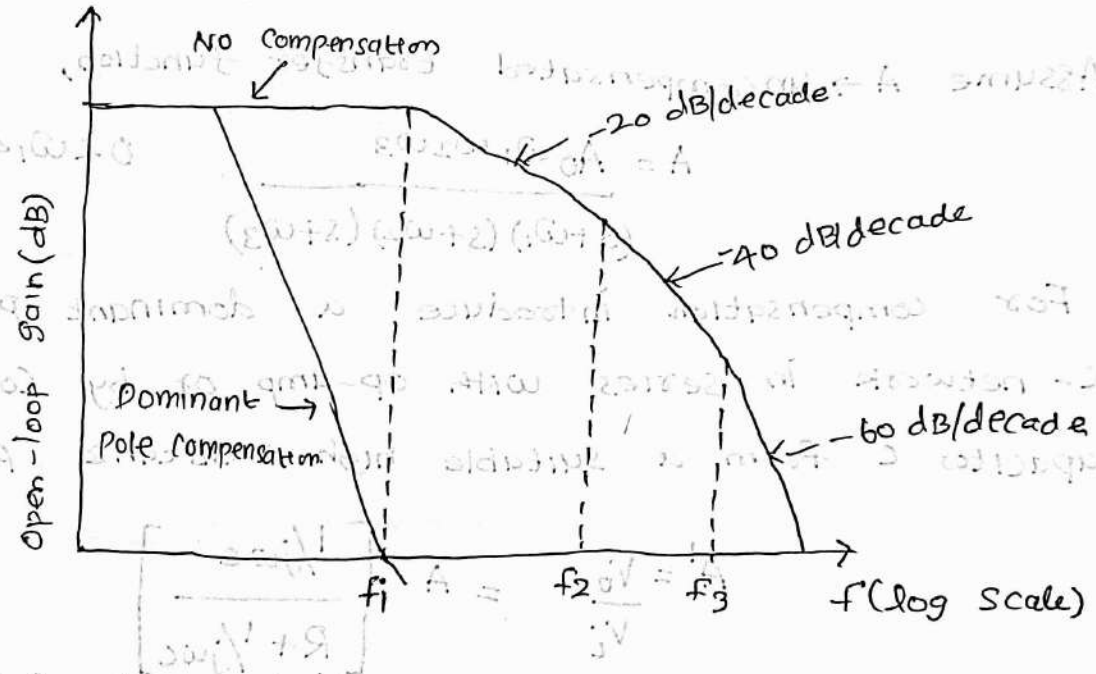
$$A' = \frac{A_0}{(1+jf/f_d)(1+jf/f_1)(1+jf/f_2)(1+jf/f_3)}$$

$$f_d < f_1 < f_2 < f_3$$

* Capacitance C is selected such that the modified loop gain drops down to 0 dB with a roll-off rate as given by 20 dB/decade @ a frequency, where the poles of the uncompensated S/m transfer fn A, → contributes negligible phase shift.

* Dis-advantage: Bandwidth of op-amp ckt reduces drastically from f_1 to f_d.

* Advantage: Improved noise immunity of the S/m.



Pole-Zero (lag) Compensation

* Uncompensated transfer function A → altered by adding both pole and zero.

* Zero should be @ higher frequency than pole.

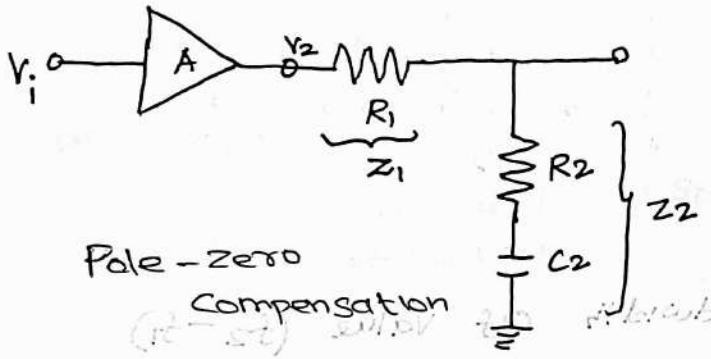
Tr. fn of compensating n/w alone,

$$\frac{V_0}{V_2} = \frac{Z_2}{Z_1 + Z_2} = \frac{R_2 + 1/j\omega C_2}{R_1 + R_2 + 1/j\omega C_2}$$

where $Z_1 = R_1$ $\quad Z_2 = \frac{1}{j\omega C_2} + R_2$

$$\frac{V_o}{V_2} = \frac{1 + j\omega R_2 C_2}{1 + j\omega (R_1 + R_2) C_2} = \frac{1 + (jf/f_1)}{1 + (jf/f_0)}$$

$$f_1 = \frac{1}{2\pi R_2 C_2} \qquad f_0 = \frac{1}{2\pi (R_1 + R_2) C_2}$$



* Zero @ first corner frequency → Cancel the effect of Pole at f_1.

* Pole of compensating n/w $f_0 = \frac{\omega_0}{2\pi}$ is selected. So that the transfer function 'A' passes thru 0 dB @ the 2nd corner frequency f_2 of the uncompensated tr. fn A.

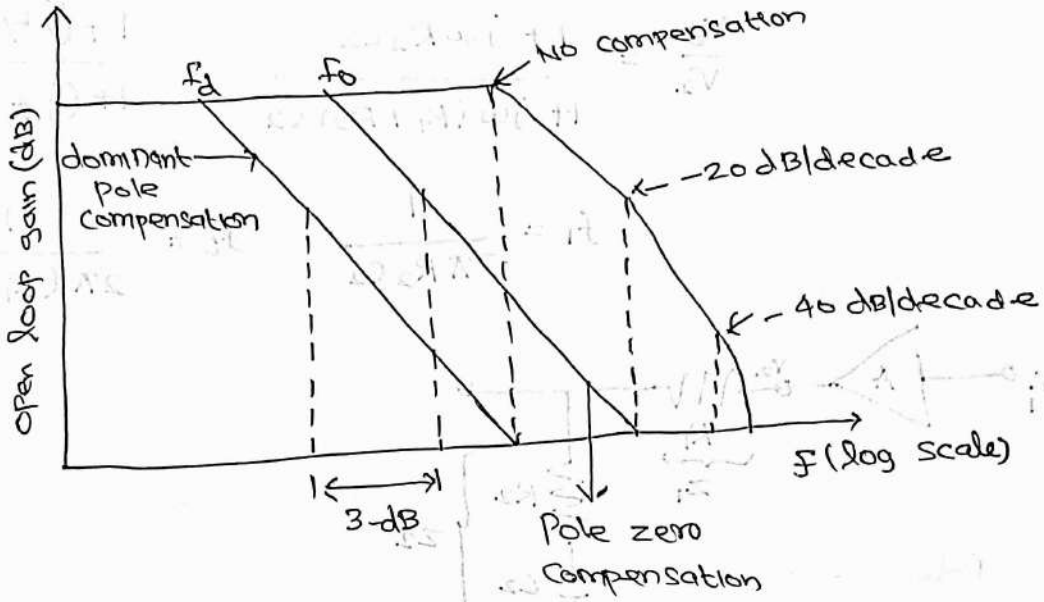
Assume, compensating n/w does not load the amplifier $R_2 >> R_1$, then overall transfer function,

$$A' = \frac{V_o}{V_i} = \frac{V_o}{V_2} \cdot \frac{V_2}{V_i} = A \frac{(1 + jf/f_1)}{(1 + jf/f_0)}$$

$$= \frac{A_0 (1 + jf/f_1)}{(1 + jf/f_0)(1 + jf/f_1)(1 + jf/f_2)(1 + jf/f_3)}$$

$$= \frac{A_0}{(1 + jf/f_0)(1 + jf/f_2)(1 + jf/f_3)} \qquad 0 < f_0 < f_1 < f_2 < f_3$$

$R_2 >> R_1$ So that $\frac{R_2}{R_1+R_2} \approx 1$



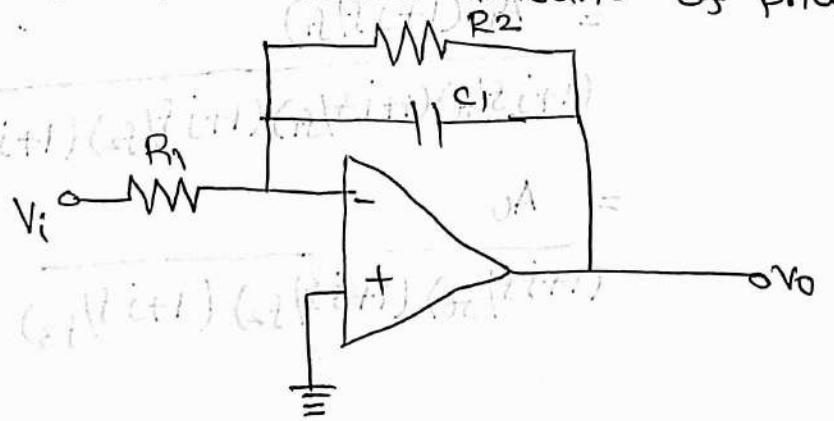
* Advantage: Improved Bandwidth of value $(f_2 - f_1)$

* dis-advantage: size of compensation capacitance is large, standard IC op-amps have Xternal pins provided to facilitate the external component connection.

This drowback eliminated in miller effect compensation method.

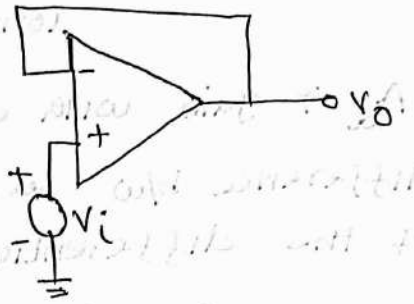
Miller effect compensation

* Combination of C_1 and R_1 behaves as phase-lead n/w in the feedback loop of op-amp. Thus C_1 and R_1 introduce a phase lead to cancel some amount of phase-lag in loop.



Voltage follower : Basic application of Op-Amp

* If Non-Inverting amplifier, $R_f = 0$, $R_1 = \infty$ we get Voltage follower.



* output voltage = Input voltage
(Both magnitude and phase)
Output voltage follows the input voltage

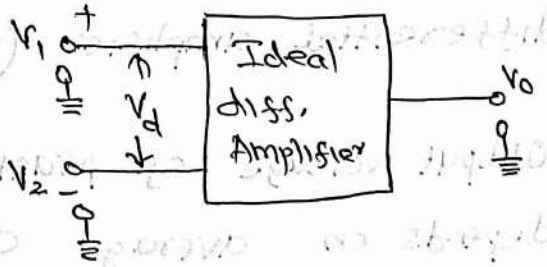
* used as buffer for impedance matching (to connect a high impedance source to a low impedance load)

* unity gain ckt → Z_i = high
$Z_o = 0$. draws negligible current from source.

Differential Amplifier

* Amplifies the difference b/w two input voltage sgl.

V_o : Output sgl
V_1 V_2 : input signal
V_d : difference input voltage
$V_1 - V_2$



$$\left.\begin{aligned} V_o &\propto (V_1 - V_2) \\ V_o &\propto V_d \end{aligned}\right] \text{Ideal differential amplifier.} \quad \text{— (1)}$$

* Each sgl is measured with respect to ground

Differential Gain A_d

From ① → $V_o = A_d(V_1 - V_2)$

↓

Constant of proportionality

A_d → gain with which differential amplifier amplifies the difference b/w two input sgl. called as differential gain of the differential amplifier.

A_d = differential gain

$V_d = V_1 - V_2$ ∴ $V_o = A_d V_d$

↓

difference voltage

$$\boxed{A_d = \frac{V_o}{V_d}}$$

In terms of decibel

$$A_d = 20\log_{10}(A_d) \text{ in dB.}$$

Common mode Gain A_c

* When two i/p voltages which are equal is applied to the differential amplifier. $(V_1 = V_2)$ then o/p voltage $V_o = 0$.

* Output voltage of practical differential amplifier depends on average common level of two inputs.

$V_c = \frac{V_1 + V_2}{2}$ ↓ average level of two i/p sgl.

Called as common mode signal.

* differential amplifier output ∝ common mode sgl V_c

$$V_o = A_c V_c$$

$$\therefore V_o = A_d V_d + A_c V_c$$

For ideal differential amplifier,

A_d = infinite, while common mode gain = 0.

This ensure $V_1 = V_2$; $V_o = 0$

* pratically $A_c \neq 0$, A_d = very large. At this stage One important parameter called Common mode Rejection Ratio (CMRR)

Common mode Rejection Ratio (CMRR)

* Common mode configuration: When same voltage is applied to both inputs

* many disturbance sgl (i) noise → appear as input sgl to both the inputs of diff. amplifier. Such sgl should be rejected by diff. amplifier.

* CMRR: ability of a differential amplifier to reject a common mode sgl.

$$CMRR, \rho = \left| \frac{A_d}{A_c} \right|$$

Ideally, $A_c = 0$, CMRR = ∝ (infinite). CMRR in dB

$$\text{CMRR in dB} = 20 \log \left| \frac{A_d}{A_c} \right| \text{ dB}$$

$$V_o = A_d V_d + A_c V_c$$

$$= A_d V_d \left[1 + \frac{A_c V_c}{A_d V_d} \right]$$

$$= A_d V_d \left[1 + \frac{1}{(A_d/A_c)} \frac{V_c}{V_d} \right]$$

$$V_o = A_d V_d \left[1 + \frac{1}{\text{CMRR}} \cdot \frac{V_c}{V_d} \right]$$

Output ∝ difference sgl. Common mode component is rejected.

CMRR is large, V_c and V_d → present.

Features of diff amplifier

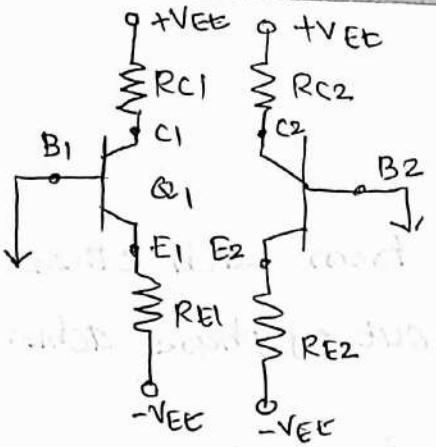
1. High voltage gain
2. low common mode gain
3. High CMRR
4. Two input terminals
5. Large Bandwidth
6. High input impedance
7. Low output impedance
8. Low offset voltage ; current.

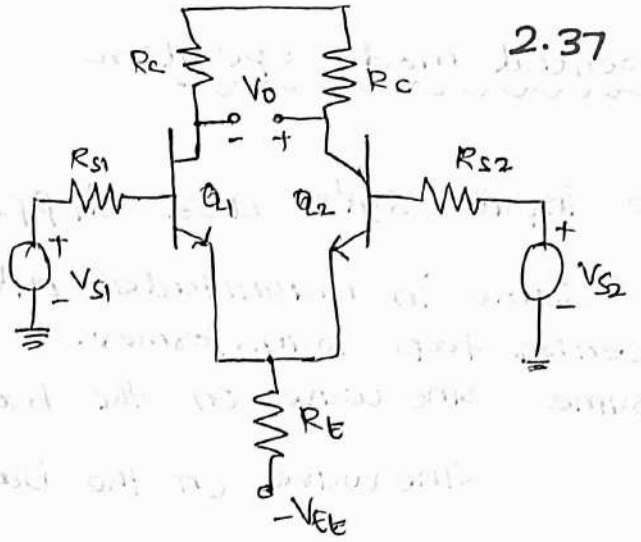
Transistorised differential amplifier

* Two emitter biased circuit
  ↳ Identical emitter biased circuit.

Q_1 , Q_2 = Transistor (exactly matched characteristic)

$R_{C1} = R_{C2}$ $R_{E1} = R_{E2}$ $+V_{CC} = -V_{EE}$





* Connections:

(a) E_1 of Q_1 to E_2 of Q_2

R_{E1}, R_{E2} becomes parallel and replaced by R_E

(b) b_1 of Q_1 to V_{S1}

b_2 of Q_2 to V_{S2}

* measure supply voltage wrt ground.

Balanced output between C_1 and C_2. Emitter Coupled differential amplifier.

$R_{C1} = R_{C2} = R_C$.

* output taken blw two collector. called as balanced o/p or double ended o/p or floating o/p.

* output collector & ground, called as unbalanced o/p / single ended o/p.

Two modes of ckt operation

(a) Differential mode

(b) Common mode

* Two input sgl's are different from each other.

Same in magnitude but 180° out of phase achieved by centre tap transformer.

* Assume sine wave on the base Q_1 is positive

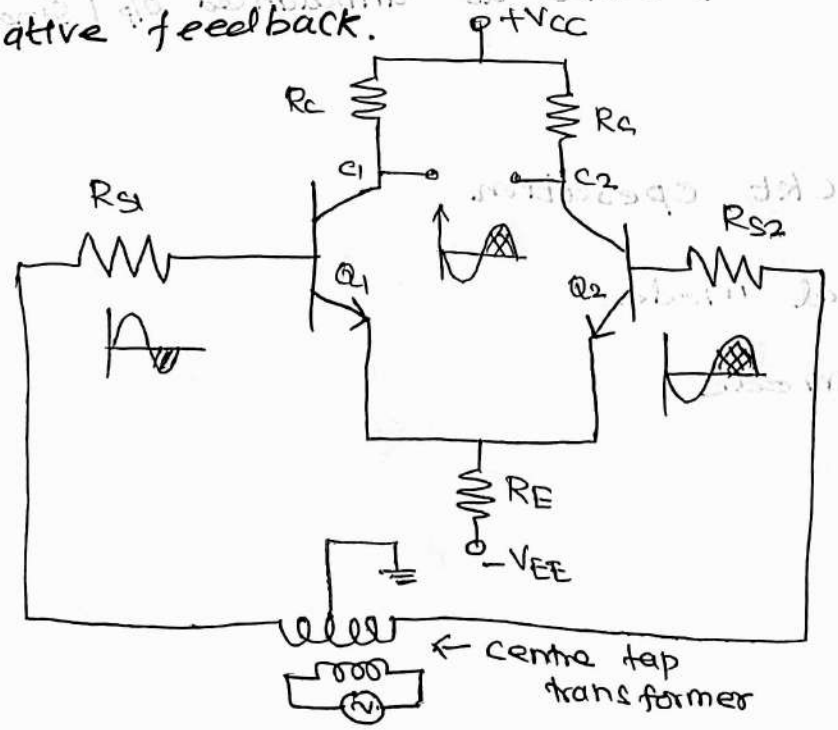
sine wave on the base Q_2 is negative

* Positive sgl on base of Q_1, an amplified negative going sgl develops on the collector Q_1, R_E also increases Hence Positive going wave developed across R_E

* negative sgl on base of Q_2, an amplified negative going sgl develops on ... of Q_2, positive going sgl develops across R_E bcoz of emitter follower action Q_2

* Sgl voltage across R_E, due to effect of Q_1, Q_2 are equal in magnitude and 180° out of phase due to matched pair transistor.

* Two sgl cancel each other and there is no AC sgl current flowing through the emitter resistance. R_E not introduce negative feedback.



Common mode operation

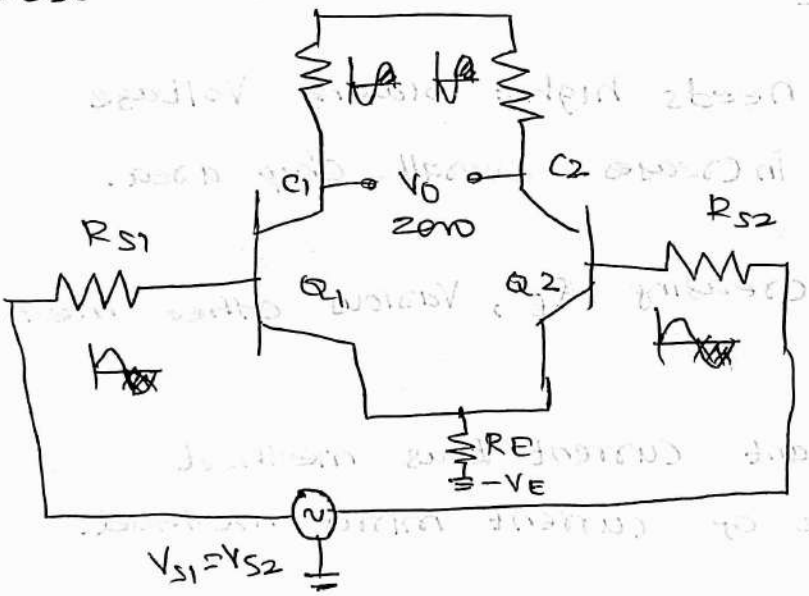
* Sgl applied to the base Q_1 and Q_2 are derived from the same source. Two Sgl's are equal in magnitude & phase.

* Sgl voltages at the bases Q_1 and Q_2 causes in-phase signal voltages to appear across R_E. which add together.

* R_E carries a Sgl current and provide a negative feedback which reduces the common mode gain of diff. amplifier.

V_o: difference b/w the two signal @ collector

V_o almost zero, negligibly small. Ideally it should be zero.



Differential amplifier circuit configurations

(i) dual input, Balanced output

(ii) dual input, Unbalanced output

(iii) Single input, balanced output

(iv) Single input, Unbalanced output

Methods of improving CMRR

* higher value of CMRR better performance

* To improve CMRR, Common mode gain A_C → reduced

* $A_C = 0$; $R_E = \infty$ because R_E introduce negative feedback in common mode operation which reduce A_C.

* Higher value of R_E, lesser value of A_C, higher value of CMRR.

A_d → not depend on R_E

* Practically R_E cannot be selected very high due

(a) Large R_E needs higher biasing voltage

(b) Large R_E increases overall chip area.

Instead of increasing R_E, various other methods are used.

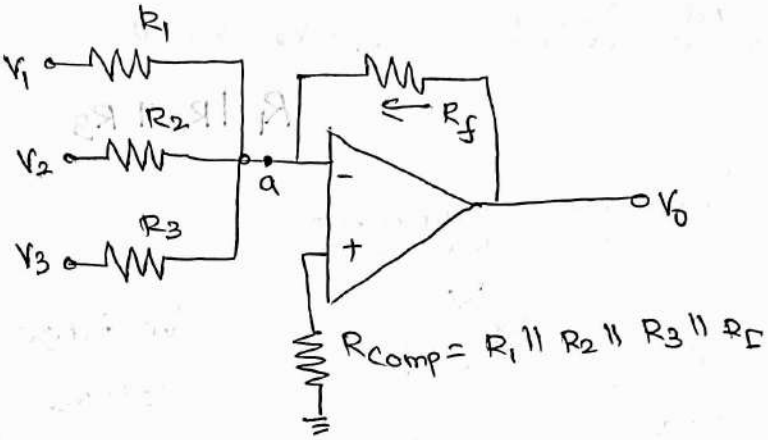
* Constant current bias method
* Usage of current mirror method.

Adder or Summing Amplifier

Op-amp may be used to design a circuit whose output → sum of several input signal. Depending upon the sign of input

(a) Inverting Summer (b) Non-Inverting Summer

Inverting Summer



3 I/p voltage : V_1, V_2, V_3

3 Resistor R_i : R_1, R_2, R_3

1 feedback Resistor.

* Open loop gain $A_{OL} = \infty$

$R_i = \infty$

∴ Input bias current = 0 ; no voltage drop across R_{comp}

non-inverting i/p terminal @ ground potential.

* Voltage at node 'a' = Zero

Apply nodal eqn by KCL at node a,

$$\frac{V_a - V_1}{R_1} + \frac{V_a - V_2}{R_2} + \frac{V_a - V_3}{R_3} + \frac{V_a - V_0}{R_f} = 0$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_0}{R_f} = 0$$

$$V_0 = -\left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right]$$

Special case : $R_1 = R_2 = R_3 = R_f$

$$\therefore V_o = -(V_1 + V_2 + V_3)$$

V_o = inverted sum of i/p sgl

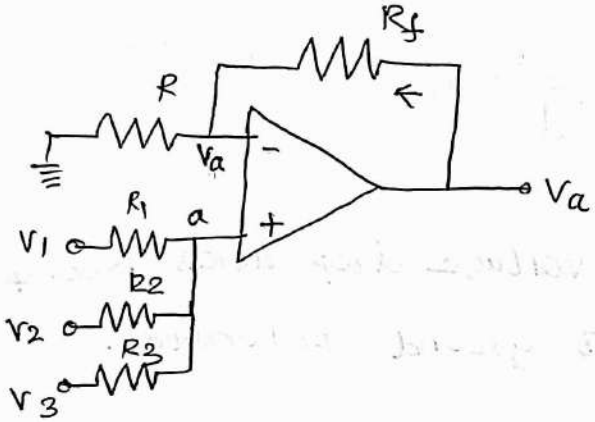
$$\therefore V_o = -\left(\frac{V_1 + V_2 + V_3}{3}\right) \quad \text{if } R_1 = R_2 = R_3 = 3R_f$$

Thus the output is the average of i/p sgl.

To find R_{comp} : $V_1 = V_2 = V_3 = 0$

$$R_i = R_1 \| R_2 \| R_3 \qquad \therefore R_{comp} = R_i \| R_f$$

Non-Inverting summer



Voltage @ (-) input terminal be V_a

Voltage @ (+) input terminal V_a.

Node eqn @ a,

$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = 0$$

$$V_a\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$$

$$V_a = \frac{(V_1/R_1) + (V_2/R_2) + (V_3/R_3)}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}$$

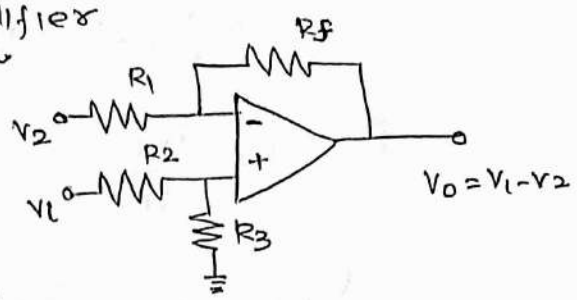
The o/p amp and two resistor R_f and R constitute Non-inverting amplifier,

$$V_o = \left(1 + \frac{R_f}{R}\right) V_a$$

$$\therefore V_o = \left(\frac{V_1/R_1 + V_2/R_2 + V_3/R_3}{1/R_1 + 1/R_2 + 1/R_3}\right)\left(1 + \frac{R_f}{R}\right)$$

$R_1 = R_2 = R_3 = R = R_f/2$ then $V_o = V_1 + V_2 + V_3$.

Subtractor or difference amplifier



* Basic differential amplifier used as subtractor
* Assume all resistors are equal
$$R_1 = R_2 = R_3 = R_f$$
* O/p voltage determined by superposition theorem.

$V_2 = 0$ ∴ V_2 is grounded then V_{o1} due to V_1 alone

$$V_{o1} = \frac{V_1}{2}\left(1 + \frac{R}{R}\right) = V_1$$

Similarly $V_1 = 0$, V_{o2} due to V_2 alone

$$V_{o2} = -V_2$$

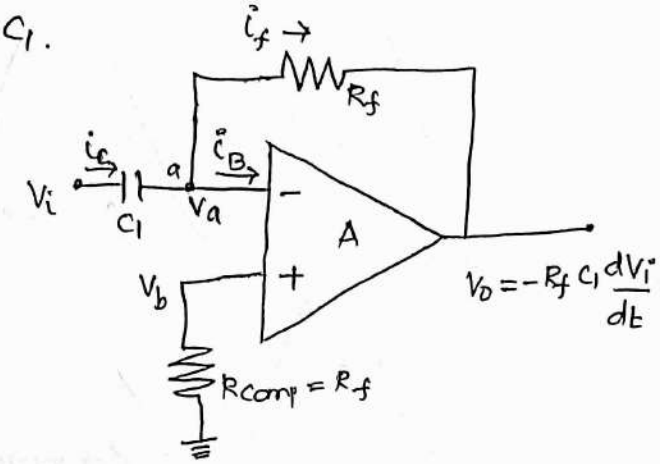
$$V_o = V_{o1} + V_{o2} = V_1 - V_2$$

This act as difference amplifier with unity gain.

Differentiator

* circuit in which o/p voltage is differentiation of input voltage. This operation is useful to find rate at which a sgl varies with time.

Ideal Differentiator: constructed from a basic inverting amplifier if R_1 is replaced by C_1.



Apply KCL at node a,

$$i_C = i_B + i_f$$

$$i_B = 0,$$

$$i_C = i_f$$

$$i_C = C_1 \frac{d}{dt}(V_i - V_a)$$

$$i_C = C_1 \frac{dV_i}{dt}$$

$$C_1 \frac{d}{dt}(V_i - V_a) = \frac{V_a - V_o}{R_f} \qquad V_a = V_b = 0$$

$$C_1 \frac{dV_i}{dt} = -\frac{V_o}{R_f} \qquad \therefore V_o = -R_f C_1 \frac{dV_i}{dt}$$

Thus the output voltage V_o is equal to $R_f C_1$ times the derivative of input voltage. The negative sign indicates 180° phase shift of the output wrt input signal.

* V_o in frequency domain

$$V_o(s) = -R_f C_1 \, s \, V_i(s)$$

Put $s = j\omega$

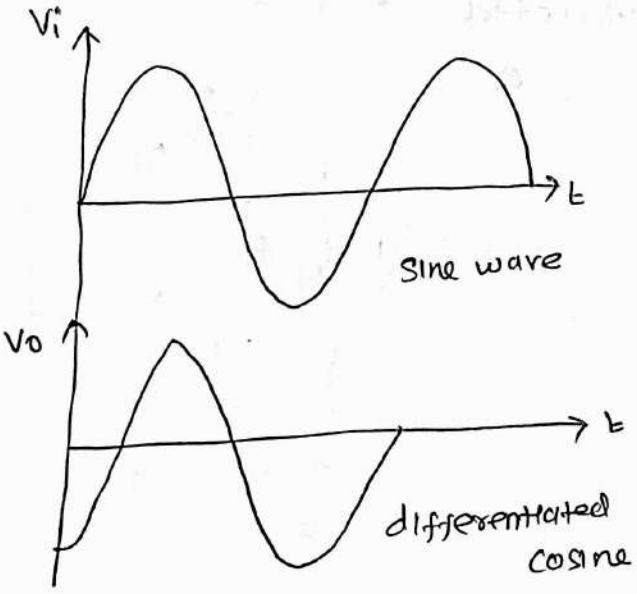
$$V_o(j\omega) = -R_f C_1 \, j\omega \, V_i(j\omega)$$

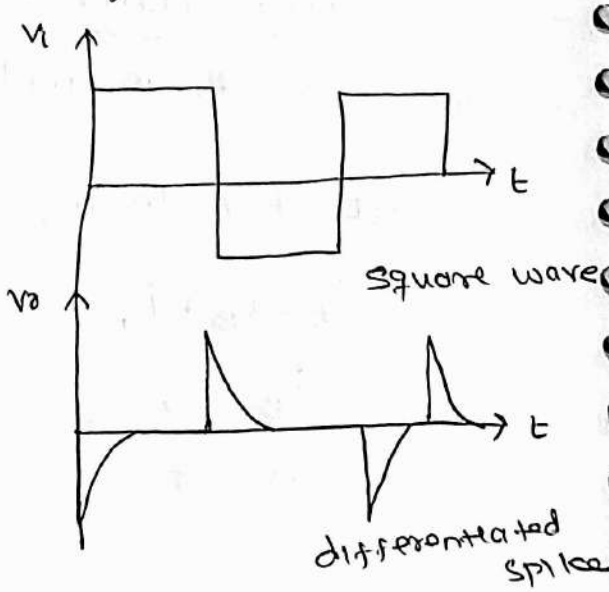
Magnitude of tr. fn

$$|A| = \left|\frac{V_o}{V_i}\right|$$

$$= |-j\omega R_f C_1| = \omega R_f C_1$$

$$|A| = \frac{f}{f_a} \qquad f_a = \frac{1}{2\pi R_f C_1}$$



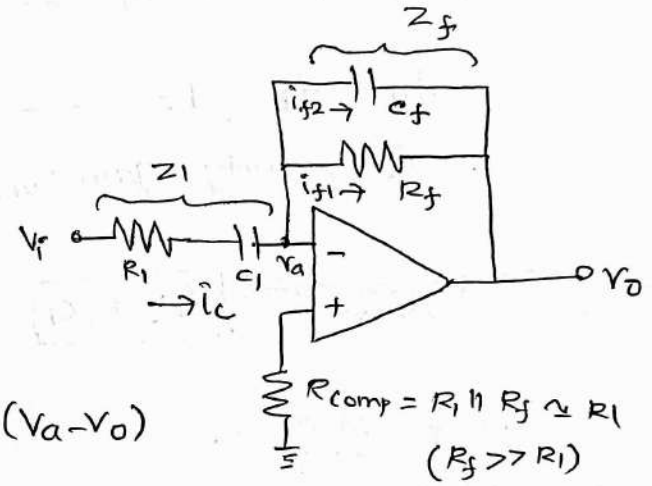


* Input noise fluctuation of small amplitude will have larger derivative. When differentiation, these sgl will generate noise, resulting in poor - signal to noise ratio.

* This drawback overcome/minimized by a series resistor with input capacitor, (constant high frequency gain).

* Stability and input impedance is overcome by a small capacitor placed parallel to R_f.

Practical Differentiator



Apply KCL at node 'a',

$$i_c = i_{f1} + i_{f2}$$

$$\frac{V_i - V_a}{R + X_C} = \frac{V_a - V_o}{R_f} + C_f \frac{d}{dt}(V_a - V_o)$$

WKT $V_a = V_b = 0$

$$\frac{V_i}{R + X_C} = \frac{-V_o}{R_f} - C_f \frac{dV_o}{dt}$$

Taking laplace transform

$$\frac{V_i(s)}{R + \frac{1}{sC_1}} = -\frac{V_o(s)}{R_f} - s C_f V_o(s)$$

$$V_i(s) \frac{sC_1}{1 + sC_1R_1} = -V_o(s)\left(\frac{1}{R_f} + sC_f\right)$$

$$\frac{V_o(s)}{V_i(s)} = -\frac{sC_1R_f}{(1 + sR_fC_f)(1 + sC_1R_1)}$$

Let $R_f C_f = R_1 C_1$

$$\frac{V_0(s)}{V_i(s)} = \frac{-sR_f C_1}{(1+sR_1C_1)^2} = \frac{-sR_f C_1}{(1+j\, f/f_c)^2} \qquad f_b = \frac{1}{2\pi R_1 C_1}$$

∴ Gain increases at +20 dB/decade for $f < f_b$

decreases at −20 dB/decade for $f > f_b$

This 40dB/decade change in gain is caused by R_1C_1 & R_fC_f

For basic differentiator, freq. response would have increased continuously @ a rate of 20dB/decade even beyond f_b.

$f_a < f_b < f_c$ ⟶ Gain @ high freq reduced by avoid high freq. noise and stability problem

$f_c \rightarrow$ unity gain band width

Good Differentiator $T_1 \geq R_f C_1$

Steps to design practical differentiator

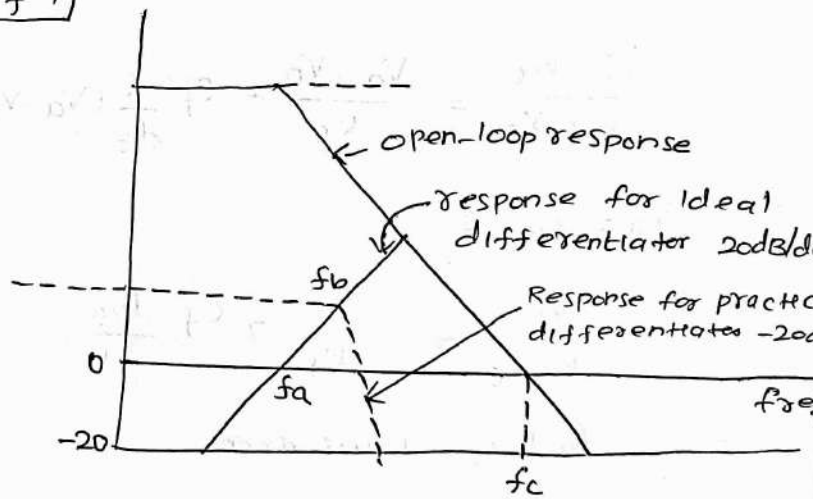
(i) choose f_a as the highest freq of i/p sgl

(ii) Choose $C_1 < 1\mu F$ and calculate R_f

(iii) Choose $f_b = 10 f_a$, ensure $f_a < f_b$

(iv) Calculate R_1, C_f from $R_1C_1 = R_fC_f$

(v) $R_{comp} = R_1 \| R_f$



frequency response

Application

(i) wave shaping ckt

(ii) Convert triangular to square wave

(iii) edge detector in FM demodulator

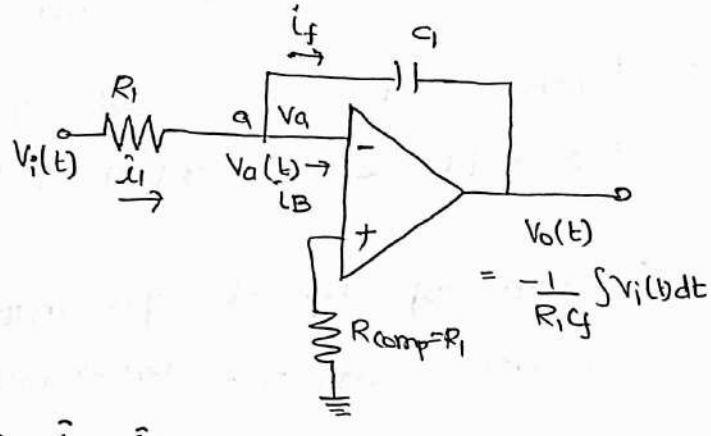
Integrator

↳ Output waveform is the time integral of input voltage

"Integrating amplifier"

Ideal Integrator

Basic inverting amplifier can be used R_f replaced by C_f.



Apply KCL @ node 'a',

$$i_1 = i_B + i_f$$

i_B is negligibly small, $\therefore i_1 = i_f$

$$\left[i = C \frac{dv}{dt} \right.$$

$$\frac{V_i(t) - V_a(t)}{R_1} = C_f \frac{d}{dt} (V_a(t) - V_o(t))$$

Gain (A_V) is large, $V_a(t) = V_b(t) = 0$

$$\frac{V_i(t)}{R_1} = C_f \frac{d}{dt} (-V_o(t)) \qquad \left[\frac{dV_o}{dt} = -\frac{1}{R_1 C_f} V_i \right]$$

Integrate on both sides,

$$\int_0^t \frac{V_i(t)}{R_1} dt = \int_0^t C_f \frac{d}{dt} (-V_o(t)) dt$$

$$\int_0^t \frac{V_i(t)}{R_1} dt = -C_f V_o(t) + V_o(0)$$

$$V_o(t) = \frac{-1}{R_1 C_f} \int_0^t V_i(t) dt + V_o(0)$$

$V_o(0)$ = integration constant and proportional to the value of $V_o(t)$ at $t = 0$.

$\therefore V_0 \propto$ negative integral of V_i

$$V_0 \propto \frac{1}{\text{time constant of } R_1C_f}$$

* Presence of (−)ve sign so, inverting integrator.
* $R_{comp} = R_1$ connected to (+) input terminal to minimize the effect of input bias current
* Gain of ideal op-amp $= \infty$, so, time constant → large, makes perfect integration.

In frequency domain

$$V_0(S) = \frac{-1}{SR_1C_f} V_i(S)$$

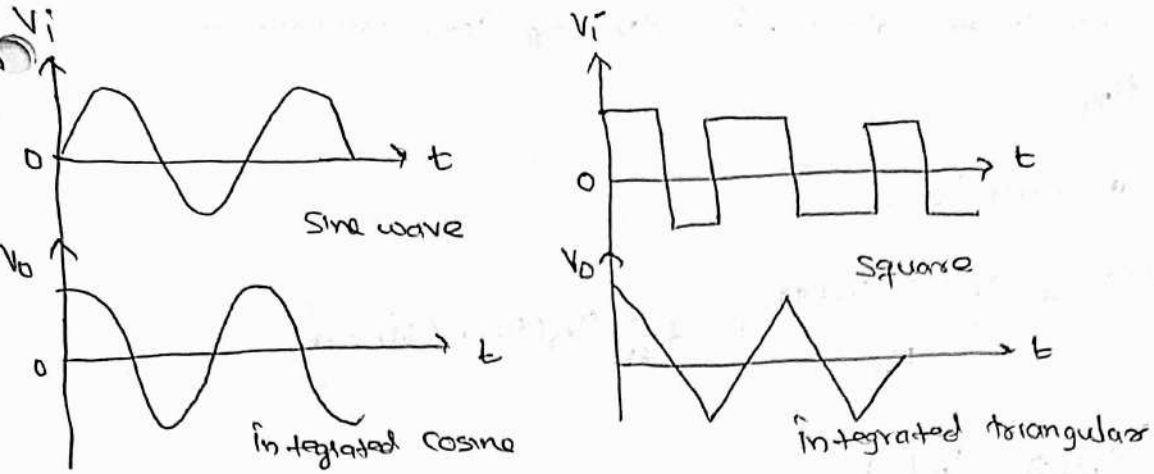
Let, $S = j\omega$ in steady state

$$V_0(j\omega) = \frac{-1}{j\omega R_1C_f} V_i(j\omega)$$

$$|A| = \left|\frac{V_0(j\omega)}{V_i(j\omega)}\right| = \left|\frac{j}{\omega R_1C_f}\right|$$

$$= \frac{1}{\omega R_1C_f}$$

* At $\omega = 0$, gain $= \infty$
* capacitor acts as an open ckt, no negative feedback thus gain $= \infty$
* frequency ↑, gain of integrator ↓



* Absences of i/p sgl, the offset voltage and I_B produces an error voltage @ output. o/p waveform distorted.

* Bandwidth → very small ; used for very small range of i/p frequency

* Small dc offset @ input cause continuous charging of feedback capacitor that results o/p drift into +ve / -ve saturation.

Practical Integrator

* A resistor is placed in parallel with the integrator capacitor to minimize the effect of error voltage.

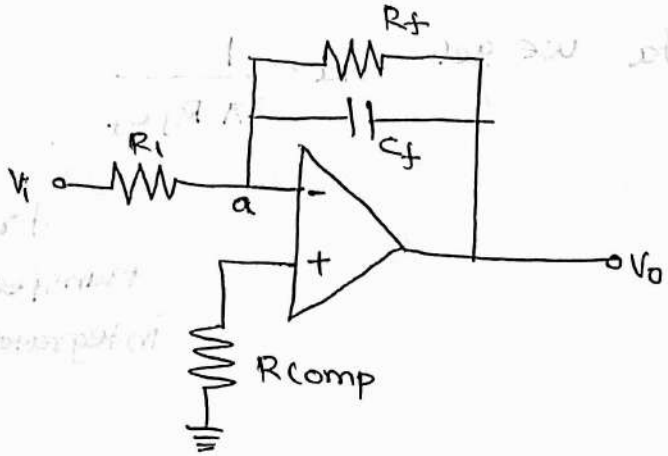
* Parallel combination of R_f and C_f dissipates power, called as a lossy integrator.

* Gain of integrator @ low frequency is limited to avoid any saturation problem.

$R_{comp} = R_1 \parallel R_f$

$R_f >> R_1$

$R_{comp} = R_1$



* R_f provides dc stabilization, by limiting low frequency gain to $-R_f/R_1$

Nodal eqn at node 'a',

$$\frac{V_a(s)-V_i(s)}{R_1} + \frac{V_a(s)-V_0(s)}{R_f} + sC_f \frac{d}{dt}(V_a(s)-V_0(s)) = 0$$

$V_a(s) = 0$

$$\frac{V_i(s)}{R_1} + \frac{V_0(s)}{R_f} + s C_f V_0(s) = 0$$

$$V_0(s)\left[\frac{1}{R_f} + sC_f\right] = -\frac{V_i(s)}{R_1}$$

$$V_0(s) = -\frac{R_f}{(1+sC_f R_f)} \frac{V_i(s)}{R_1} = -\frac{V_i(s)}{sR_1C_f + R_1/R_f}$$

Sub $j\omega = s$, the transfer function,

$$|A| = \left|\frac{V_0}{V_i}\right| = \frac{1}{1-\left(j\omega R_1 C_f + \frac{R_1}{R_f}\right)} = \frac{1}{\sqrt{\omega^2 R_1^2 C_f^2 + \frac{R_1^2}{R_f^2}}}$$

$$|A| = \frac{R_f/R_1}{\sqrt{1+(\omega_{R_f} C_f)^2}}$$

R_f = Very large, lossy integrator become ideal integrator

$f = f_a$ we get $f_a = \frac{1}{2\pi R_f C_f}$ $f_b = \frac{1}{2\pi R_1 C_f}$

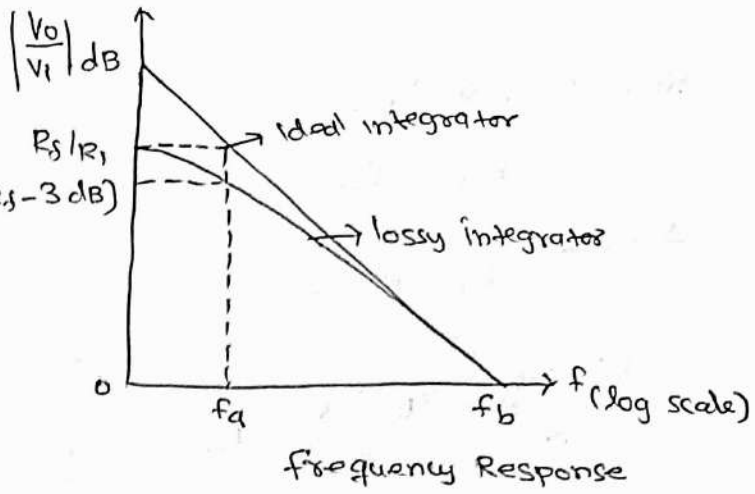
↓

frequency at which the transfer function or gain of the integrator is 1 or 0 dB.

I/p frequency < f_a, then ckt will not act as integrator, act as simple inverting amplifier.

$f = f_a$ 50% accuracy

$f = 10 f_a$ 99% accuracy

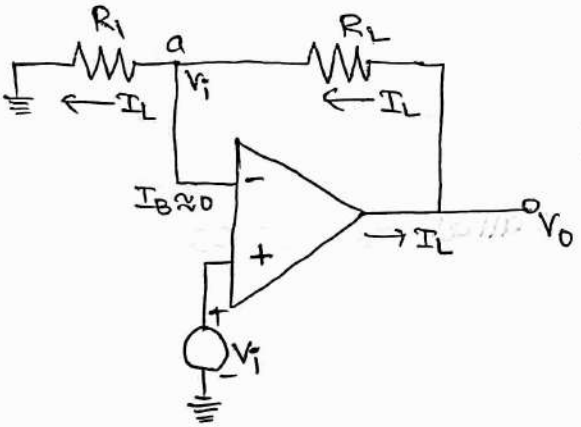


Frequency Response

Applications
* wave shaping ckts, ramp generator
* convert square wave to triangular wave
* analog to digital converter.

Voltage to Current Converter (Trans Conductance Amplifier)

Converting a voltage signal to a proportional o/p current



V to I converter floating load

* Input voltage: V_i
* output current : I_L
* R_L is floating, neither side of R_L is grounded

$$I_B = 0, \quad I_L = \frac{V_i}{R_i}$$

$$I_L \propto V_i$$

Proportionality constant is $1/R_1$. Hence the ckt is called as Transconductance amplifier, also called as Voltage Controlled Current Source (VCCS)

KCL @ node 'a',

$$I_1 + I_2 = I_L$$

Assume

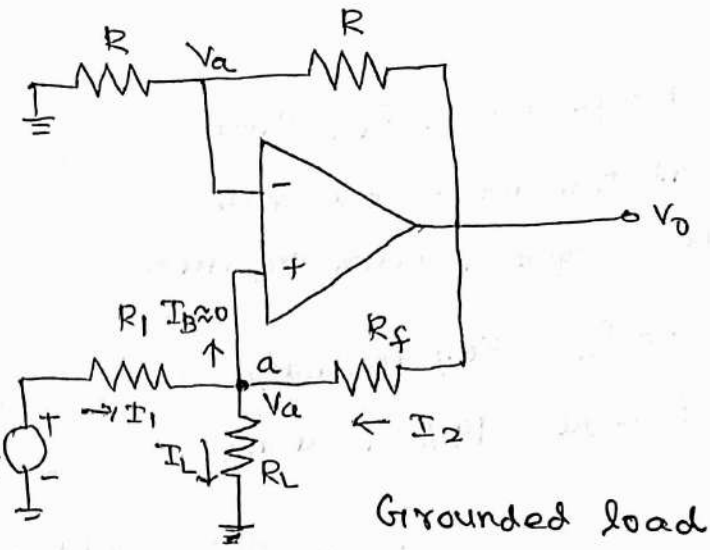
$$R_f = R_1 = R$$

$$\frac{V_i - V_a}{R} + \frac{V_0 - V_a}{R} = I_L$$

$$V_i - V_a + V_0 - V_a = RI_L$$

$$V_i + V_0 - 2V_a = RI_L$$

$$V_a = \frac{V_i + V_0 - RI_L}{2}$$



Grounded load

Gain of non-inverting op-amp $1 + R/R = 2$

$$V_0 = 2V_a$$

$$V_0 = V_i + V_0 - RI_L$$

$$I_L = \frac{V_i}{R}$$

Trans conductance $(g_m) = \frac{I_L}{V_i} = \frac{1}{R}$ Called as VCCS

Application

* Input Impedance very high, draws negligible current from source. Used in low voltage voltmeters LED and Zener testers.

Current to Voltage Converter Transresistance amplifier

Current to Voltage converter (or) Ideal Current controlled Voltage Source

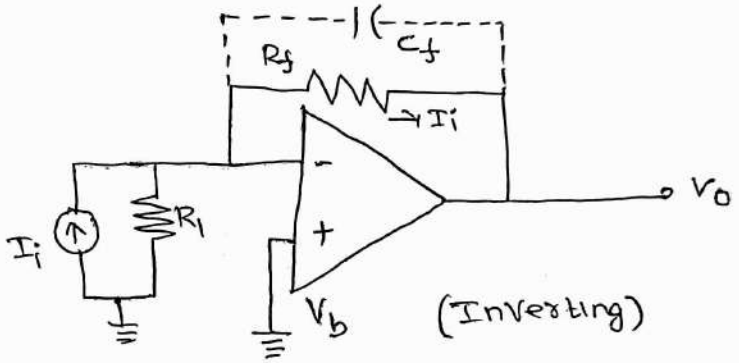
Transresistance amplifier

* V_o = constant k times the magnitude of an independent Input current

$$V_o = kI_i$$

* V_o is independent of load connected to it

* Output current from photo devices (photo cell or photo diode) can be converted to voltage by using I-V converter



* In this circuit due to virtual ground

$V_b = V_a = 0$,

current through $R_1 = 0$

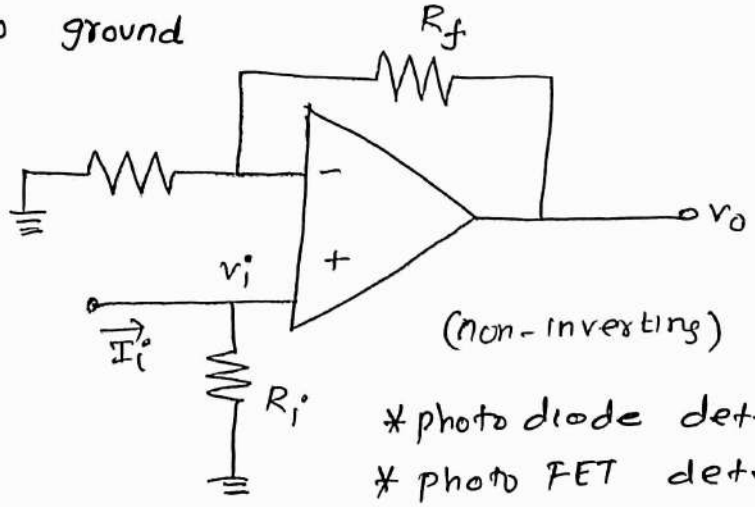
I_i flows through R_f

$$I_i = \frac{V_a - V_o}{R} = -\frac{V_o}{R}$$

$$V_o = -I_i R$$

* To reduce the high frequency and oscillations, a capacitor C_f is connected across R_f

* I_i has return path to ground



$$V_i = I_i R_i$$

$$V_o = \left[1 + \frac{R_f}{R_1}\right] V_i$$

$$V_o = \left[1 + \frac{R_f}{R_1}\right] I_i R_i$$

* photo diode detector
* photo FET detector

* Determine the output voltage of a differential amplifier for the input voltage 300 μV and 240 μV. The differential gain is 5000 and the value of CMRR is 100 and 10^5

$V_1 = 300\ \mu V \quad V_2 = 240\ \mu V \quad A_d = 5000$

$V_o = A_d V_d + A_c V_c$

$V_d = (300 - 240)\mu V = 60\ \mu V$

$V_c = \frac{V_1 + V_2}{2} = \frac{300 + 240}{2} = 270\ \mu V$

$CMRR = \frac{A_d}{A_c}$

(i) $100 = \frac{5000}{A_c}$

$\therefore A_c = 50$

$V_o = (5000 \times 60) + (50 \times 270)$

$= 313500\ \mu V = 313.5\ mV$

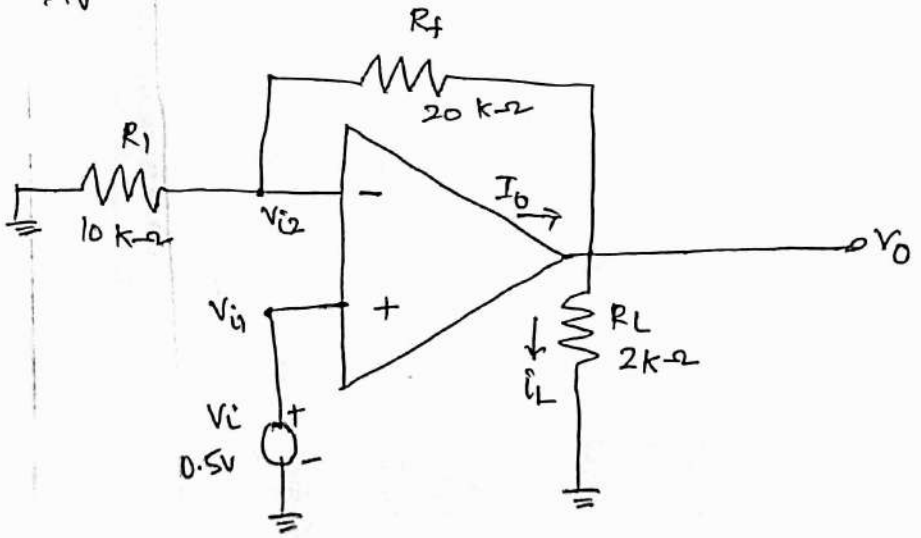
(ii) $10^5 = \frac{5000}{A_c}$

$A_c = 0.05$

$V_o = (5000 \times 60) + (0.05 \times 270)$

$= 300.0135\ mV$

* For the given non-inverting amplifier, determine V_o, I_L, I_o and A_v



$$V_o = \left[1 + \frac{R_f}{R_i}\right] V_i$$

$$= \left[1 + \frac{20 \times 10^3}{10 \times 10^3}\right] 0.5$$

$$\boxed{V_o = 1.5 \text{ volt}}$$

$$A_V = \frac{V_o}{V_i}$$

$$= \frac{1.5}{0.5}$$

$$\boxed{A_V = 3}$$

$$i_L = \frac{V_o}{R_L} = \frac{1.5}{2 \times 10^3} = 7.5 \times 10^{-4}$$

$$= \frac{15 \times 10^{-1}}{2 \times 10^3} = \boxed{0.75 \text{ mA} = i_L}$$

$$i_o = i_1 + i_L$$

$$i_1 = \frac{V_o - V_i}{R_f} = \frac{1.5 - 0.5}{2 \times 10^3} = \boxed{0.5 \text{ mA} = i_1}$$

$$i_o = 0.75 \text{ mA} + 0.5 \text{ mA}$$

$$= i_1 + i_L$$

$$\boxed{i_o = 1.25 \text{ mA}}$$