Unit - 3

Applications of Op-Amps

Instrumentation Amplifier :-

* In a number of industrial and Consumer applications, one is required to measure and control Physical quantities

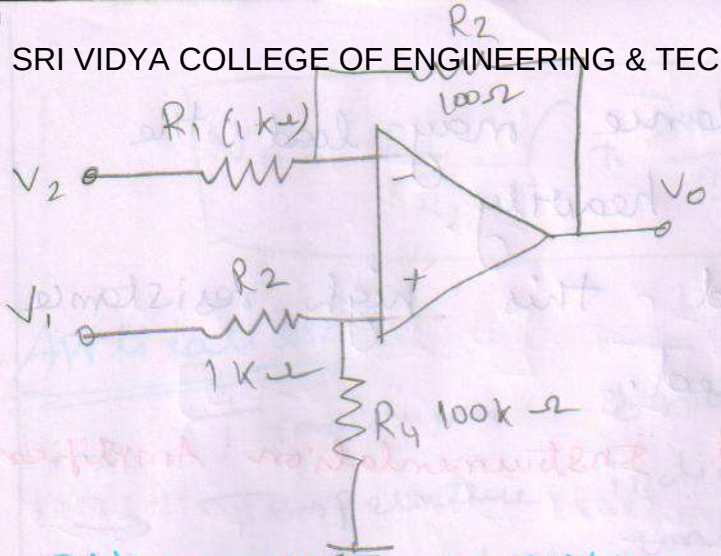
* These quantities are usually measured with the help of transducers. The output of transducers has to be amplified so that it can drive the indicator.

* This function is Perfored by an instrumentation amplifier.

The important features are

→ high gain accuracy
→ high CMRR
→ high gain Stability with low temperature coefficient.
→ low Dc offset
→ low output impedance

Op-amps uA725 to meet above requirements. Available Op-amps are AD521, AD524, AD620, AD624



Differential amplifier using single Op-Amps

from this diagram,

$$V_o = -\frac{R_2}{R_1} V_2 + \frac{1}{1+\frac{R_3}{R_4}} V_1 \left(1+\frac{R_2}{R_1}\right)$$

$$V_o = -\frac{R_2}{R_1}\left[V_2 - \frac{1}{1+\frac{R_3}{R_4}}\left(\frac{R_1}{R_2}+1\right)V_1\right] \longrightarrow 4.16$$

$$\Rightarrow \frac{R_1}{R_2} = R_3/R_4$$

$$= -\frac{R_2}{R_1}\left[V_2 - \frac{1}{1+\frac{R_1}{R_2}}\left(\frac{R_1}{R_2}+1\right)V_1\right]$$

$$= -\frac{R_2}{R_1}\left[V_2 - \frac{1}{\frac{R_2+R_1}{R_2}}\left(\frac{R_1+R_2}{R_2}\right)V_1\right]$$

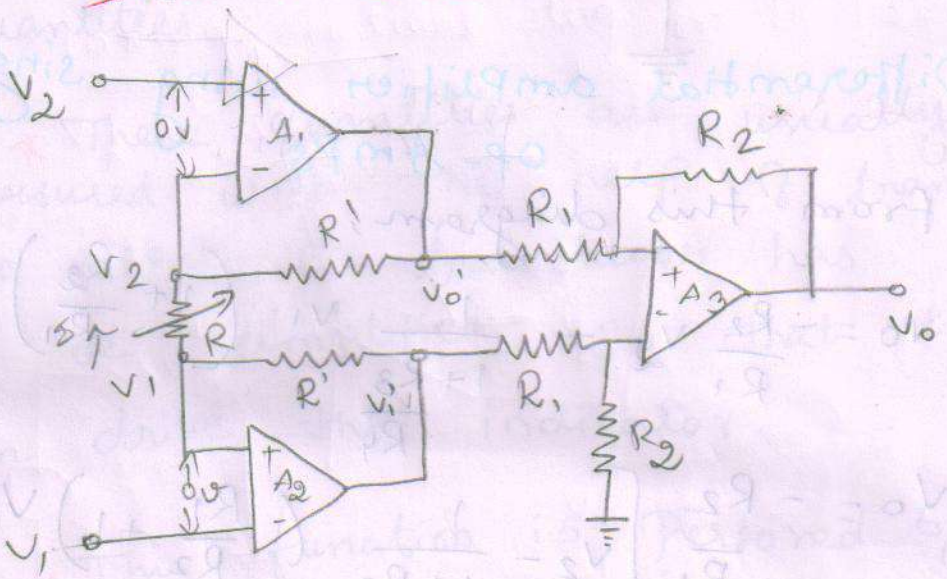
$$= -\frac{R_2}{R_1}\left[V_2 - \frac{R_2}{R_2+R_1} \times \frac{R_1+R_2}{R_2}\right]V_1$$

$$\boxed{V_o = \frac{R_2}{R_1}\left[V_1 - V_2\right]} \longrightarrow 4.17$$

→ low impedance may load the signal source heavily.

→ To avoid this high resistance buffer is used.

Improved Instrumentation Amplifier



From diagram

$$V_o = -\frac{R_2}{R_1} V_2' + \left(1+\frac{R_2}{R_1}\right)\left(\frac{R_2 V_1'}{R_1+R_2}\right)$$

$$= \frac{R_2}{R_1}(V_1' - V_2') \rightarrow 4.18$$

→ Since no current flow,

$$V_1' = R'I + V_1 = \frac{R'}{R}(V_1 - V_2) + V_1 \rightarrow 4.19$$

$$V_2' = -R'I + V_2 = \frac{-R'}{R}(V_1 - V_2) + V_2 \rightarrow 4.20$$

Substitute V_1' & V_2'

$$V_o = \frac{R_2}{R_1}\left[\frac{2R'}{R}(V_1 - V_2) + (V_1 - V_2)\right.$$

$$V_o = \frac{R_2}{R_1}\left(1+\frac{2R'}{R}\right)(V_1 - V_2)$$

Applications :

- Transducer bridge
- Temperature indicator
- temperature controller
- light intensity meter

log & Antilog Amplifier :

Log-amp can be used to compress the dynamic range of a signal.

Log Amps :

A grounded base transistor is placed in the feedback Path. Since the collector is held at virtual ground then,

$$I_E = I_S\left(e^{qV_E/kT} - 1\right)$$

$$I_E = I_C$$

$$I_C = I_S\left(e^{qV_E/kT} - 1\right)$$

Therefore

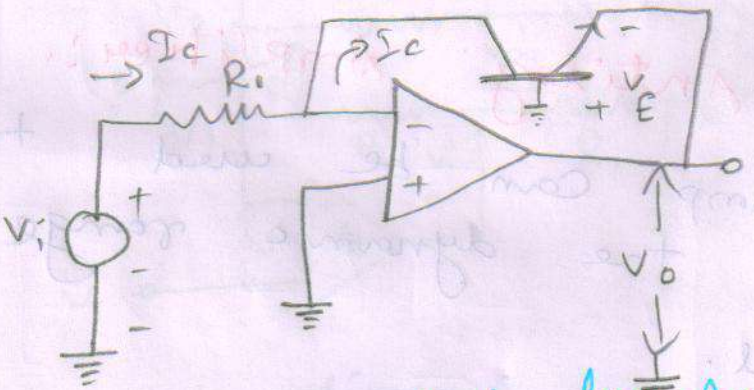
$$\frac{I_C}{I_S} = e^{qV_E/kT} - 1)$$

$$e^{qV_E/kT} = \frac{I_C}{I_S} + 1$$

$$= \frac{I_C}{I_S} \quad [\text{as } I_S \approx 10^{-13} A, \; I_C >> I_S]$$

Taking natural log on both sides

$$V_k = \frac{kT}{q} \ln \frac{I_C}{I_S}$$



Fundamental log Amp.

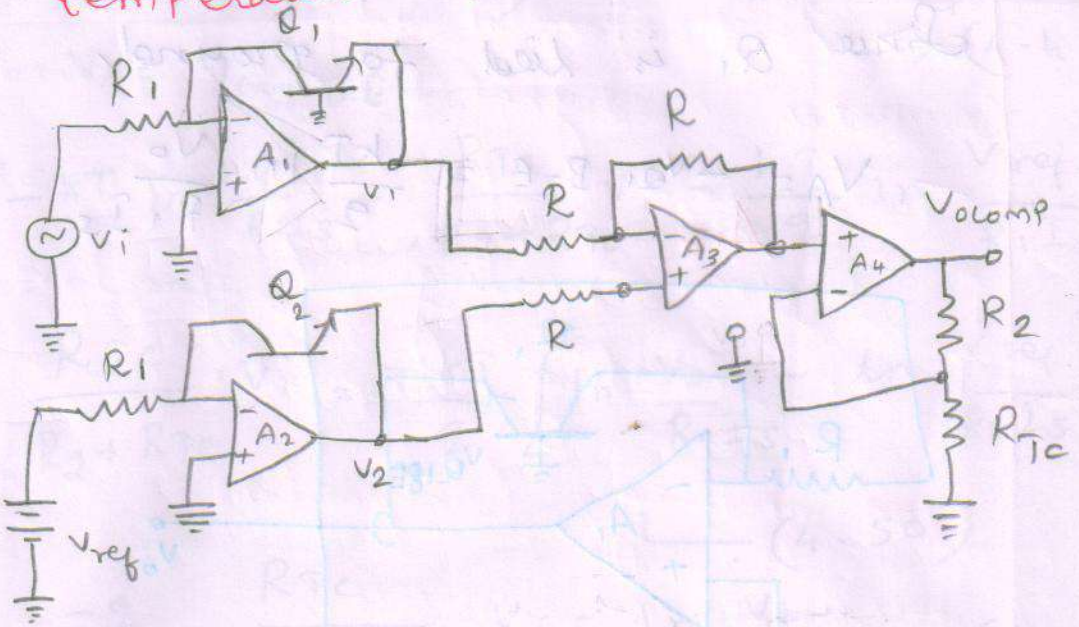
$$\text{So, } V_o = \frac{-kT}{q} \ln\left(\frac{V_i}{R_1 I_S}\right) = -\frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$$

$$\boxed{V_{ref} = R_1 I_S}$$

→ I_S varies from transistor to transistor & with temperature

To overcome this Problem two transistors are integrated close together in the same Silicon wafer.

log Amp with temperature compensation.



Assume,

$$I_{S1} = I_{S2} = I_S$$

$$V_1 = -\frac{kT}{q} \ln \frac{V_i}{R_1 I_S}$$

$$V_2 = -\frac{kT}{q} \ln \frac{V_{ref}}{R_1 I_S}$$

$$V_o = \frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$$

$$V_{ocomp} = \left(1 + \frac{R_2}{R_{TC}}\right) \frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$$

Anti log Amplifier:

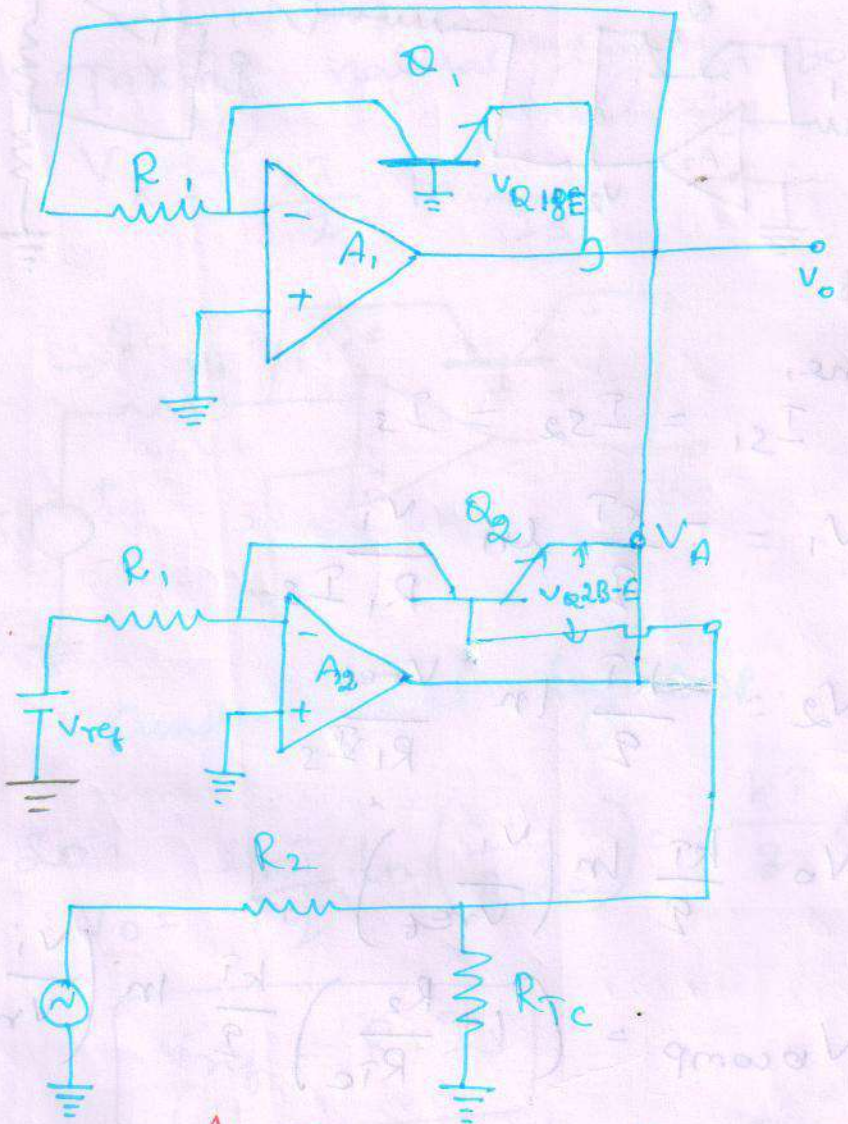
→ input V_i is fed into the temperature compensating voltage divider R_2 & R_{TC}, The base emitter voltage of Transistors

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{V_o}{R_1 I_S}\right)$$

$V_{Q2B-E} = \frac{kT}{q} \ln\left(\frac{V_o}{R_1 I_s}\right)$

Since Q_1 is tied to ground,

$$V_A = -V_{Q1\ B-E} = -\frac{kT}{q} \ln \frac{V_o}{R_1 I_s}$$



Analog Amplifier.

The Base voltage V_B & Q_2 is

$$V_B = \frac{R_{TC}}{R_2 + R_{TC}} V_i \longrightarrow (4\text{-}48)$$

voltage at the emitter is Q_2 is

$$V_{Q_2 B-E} = V_B + V_{Q_2 E-B}$$

$$V_{Q_2\,BE} = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i - \frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_S}\right)$$

→ (4.49)

$$V_A = V_{Q_2\,B.E}$$

$$-\frac{kT}{q} \ln \frac{V_o}{R_1 I_S} = \frac{R_{TC}}{R_2 + R_{TC}} V_i - \frac{kT}{q} \ln \frac{V_{ref}}{R_1 I_S}$$

$$\frac{R_{TC}}{R_2 + R_{TC}} V_i = -\frac{kT}{q} \left[\ln \frac{V_o}{R_1 I_S} - \ln \frac{V_{ref}}{R_1 I_S} \right]$$

→ (4.50)

$$-\frac{q}{kT} \frac{R_{TC}}{R_2 + R_{TC}} V_i = \ln \frac{V_o}{V_{ref}} \longrightarrow (4.51)$$

Changing natural log,

$$-k' V_i = \log_{10} \left(\frac{V_o}{V_{ref}}\right) \longrightarrow (4.52)$$

$$\frac{V_o}{V_{ref}} = 10^{-k' V_i}$$

$$V_o = V_{ref} \left(10^{-k' V_i}\right) \longrightarrow (4.53)$$

$$k' = 0.4343 \left(\frac{q}{kT}\right) \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) \longrightarrow 4.54.$$

Hence an increase in input by one volt causes the output decrease by a decade.

Filters

→ Electric filters are used in

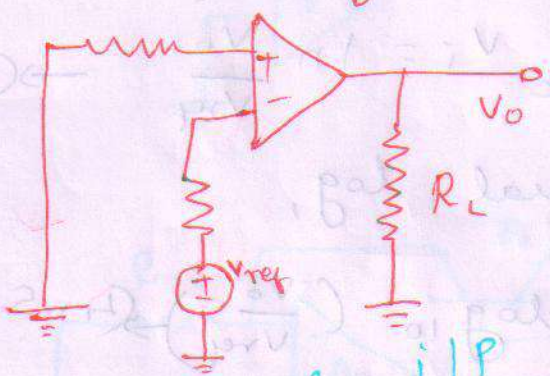
Comparators :-

→ A Comparator is a circuit which Compares a signal voltage applied.

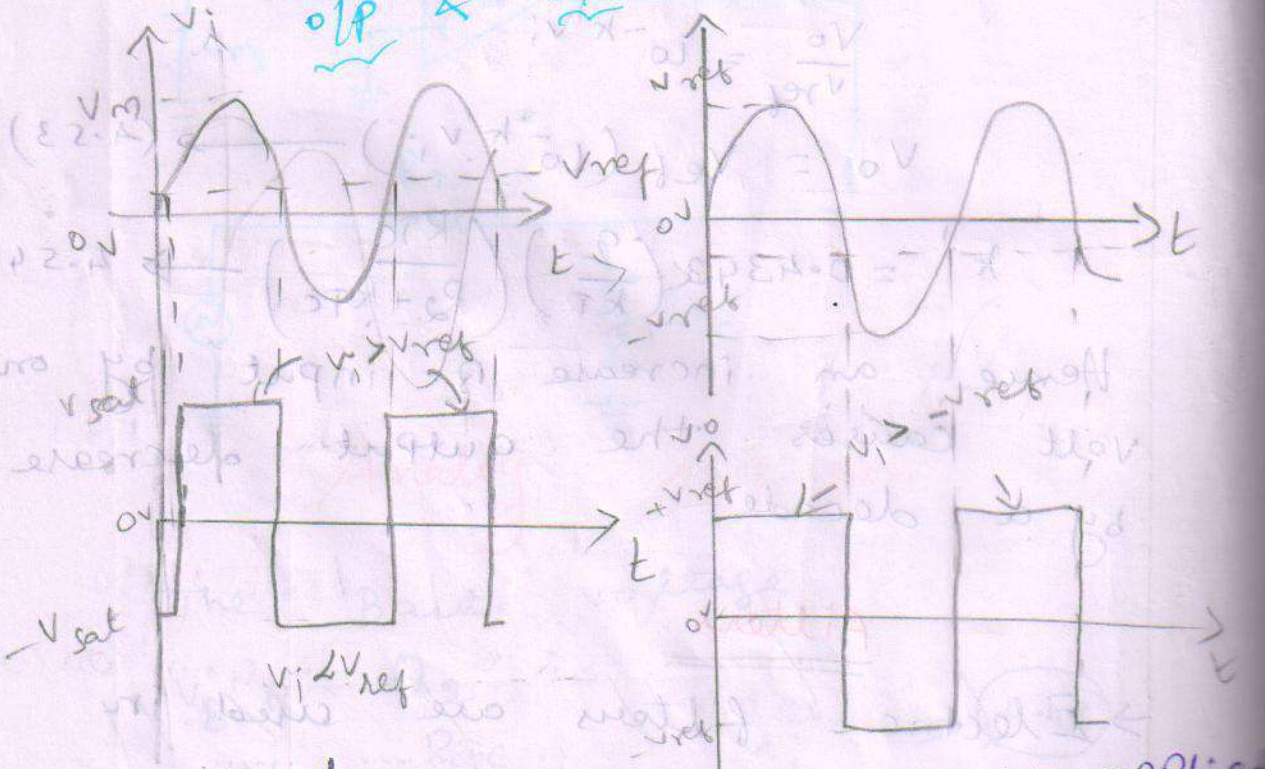
Two basic types of Comparators

1) Non inverting Comparator
2) Inverting Comparator

Non inverting Comparator



o/p & i/p waveforms:-



→ fixed ref voltage V_{ref} is applied to (−) input & v_i to (+) input.

→ It $-V_{sat}$ for $v_i < V_{ref}$ & V_o is

$+V_{sat}$ for $V_i > V_{ref}$.

Inverting Amplifier:

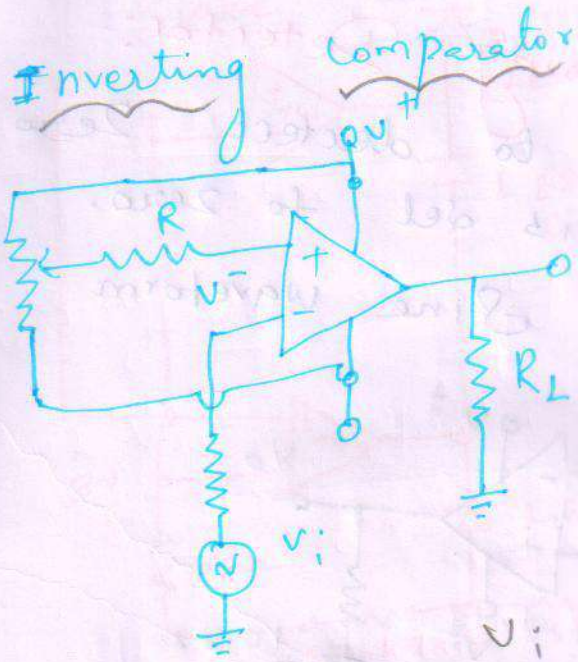
→ V_{ref} is applied to (+) input

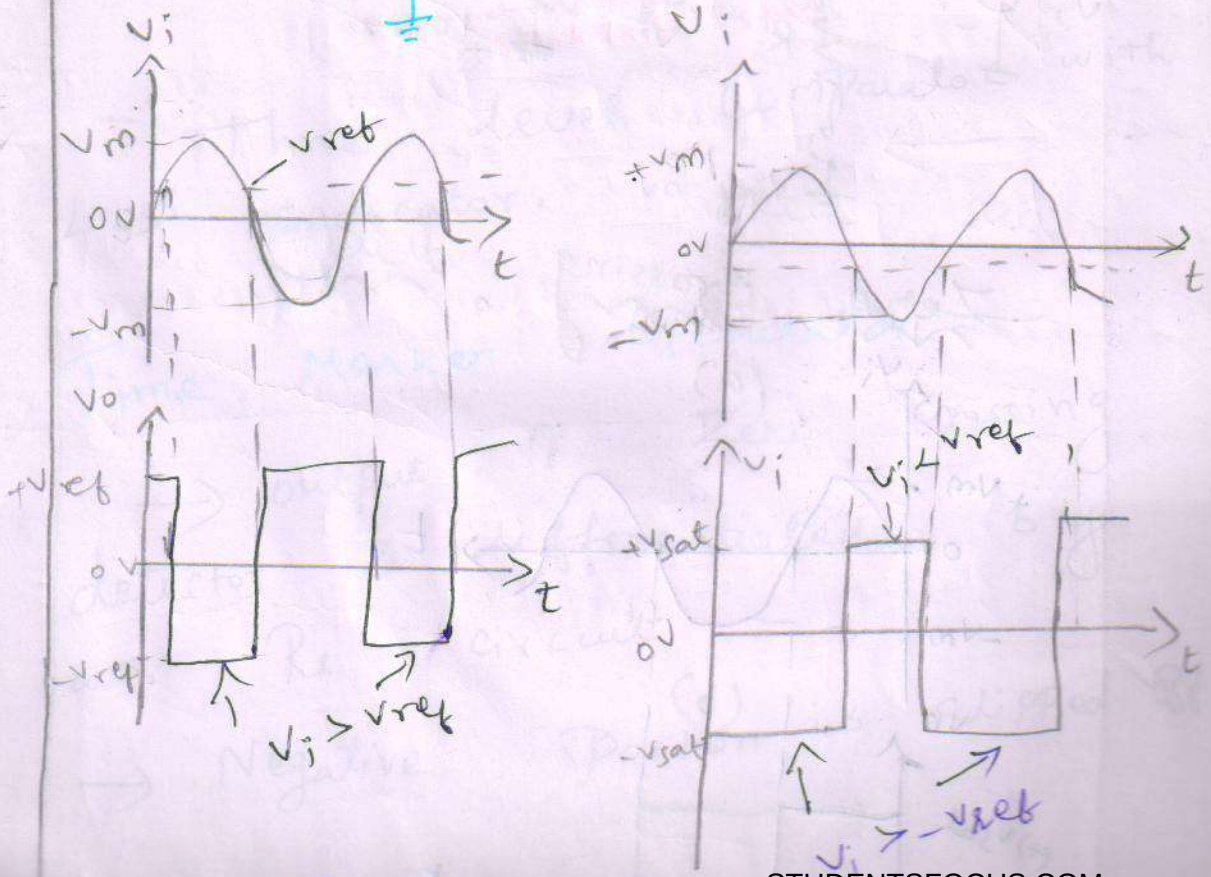
→ V_i is applied to (-) input

* Output voltage independent of Power supply.

* It can be obtained by R & back to back Zener (or) two diode.

Inverting comparator





Output waveforms

Applications of Comparator :-

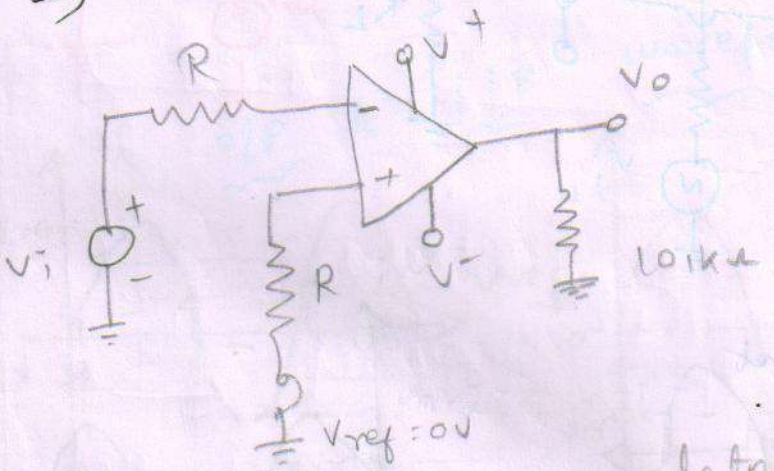
Some important application of Comparator are

1) zero crossing detector
2) window detector
3) Time Marker Generator
4) Phase meter

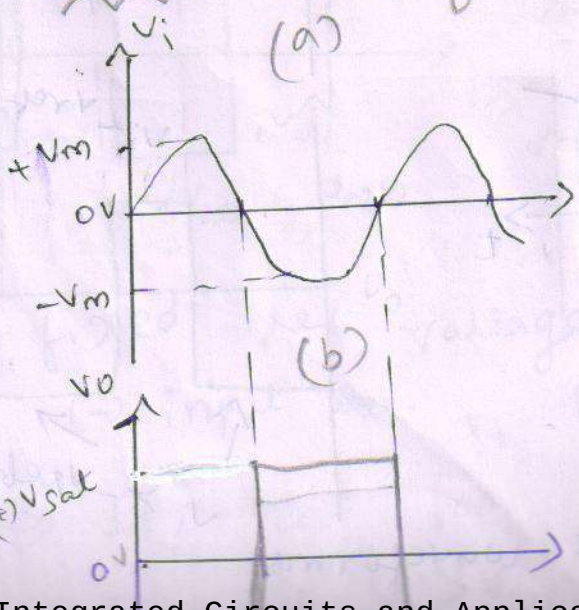
Zero Crossing Detector :-

→ used to dectect zero crossing with Vref is set to zero.

→ output Sine waveform



Zero crossing detector

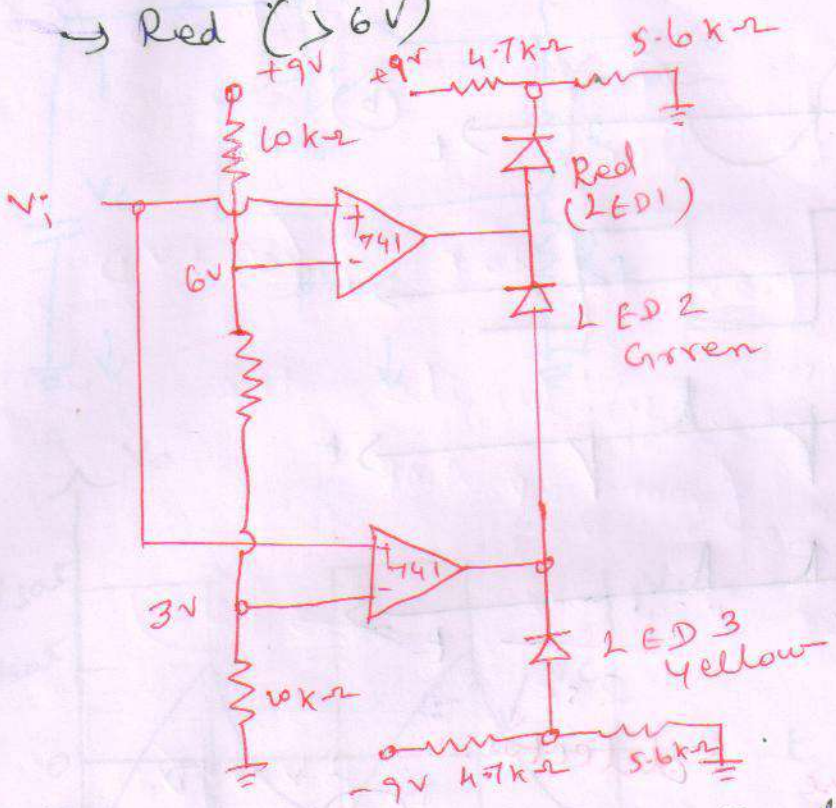


Window detector

→ Instant at which an unknown input is between two threshold levels.

→ It uses three indicators.

→ Yellow (<3V)
→ Green (3 - 6 V)
→ Red (>6V)

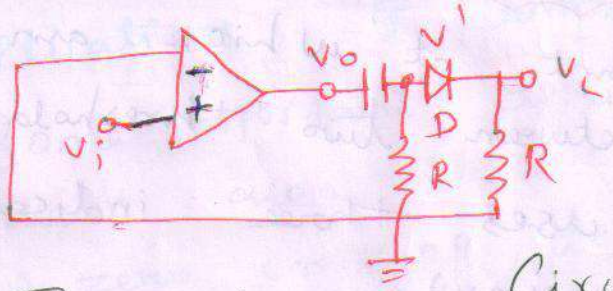


Three level comparator with LED Indicator.

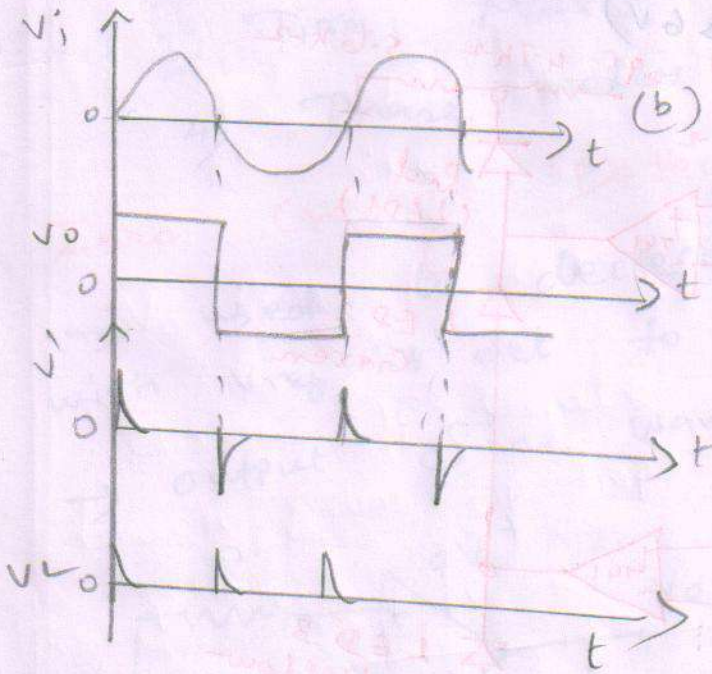
Time Marker Generator:-

→ output of Zero Crossing detector is differentiated by an RC circuit

→ Negative portion is clipped off



Time Marker Circuit



Phase detector:-

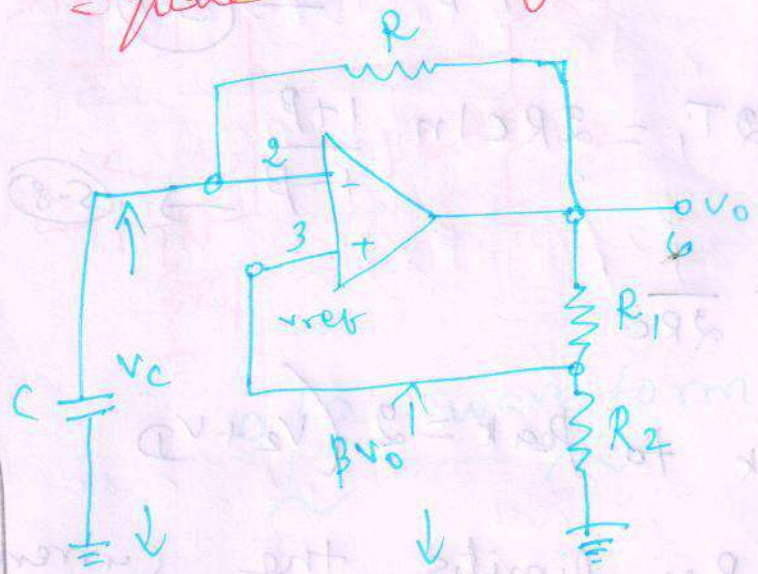
→ measured Phase angle b/w two voltages.

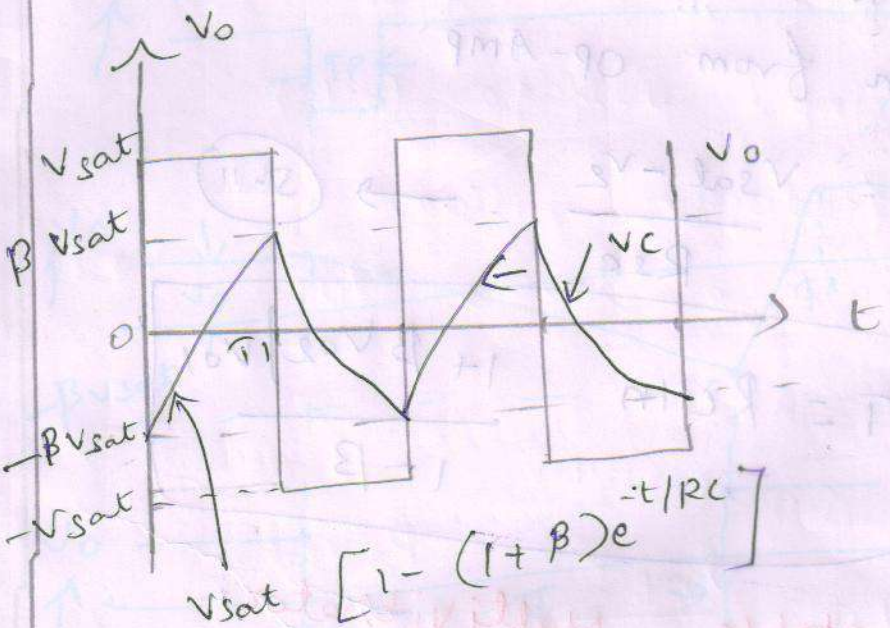
→ Time & Phase difference

Multivibrator

It is called as free running oscillator.

Square wave generator & waveforms





The voltage across the capacitor

$$v_c(t) = v_f + (v_i - v_f)e^{t/RC} \quad \rightarrow (5.4)$$

$$V_f = +V_{sat}$$

$$v_i = -\beta V_{sat}$$

$$V_c(t) = V_{sat}(-\beta V_{sat} - V_{sat})e^{-t/RC}$$

$$V_c(t) = V_{sat} - V_{sat}(1+\beta)e^{-t/RC} \quad 5.5$$

$$V_c(T_1) = \beta V_{sat} = V_{sat} - V_{sat}(1+\beta)e^{-T_1/RC}$$

→ (5.6)

$$T_1 = RC \ln \frac{1+\beta}{1-\beta} \rightarrow (5.7)$$

$$T = 2T_1 = 2RC \ln \frac{1+\beta}{1-\beta} \rightarrow (5.8)$$

$$f_o = \frac{1}{2RC}$$

V_o Peak to Peak $= 2(V_2 + V_D$

Resistor R_{sc} limits the current drawn from Op-Amp

$$I_s = \frac{V_{sat} - V_2}{R_{sc}} \rightarrow (5.11)$$

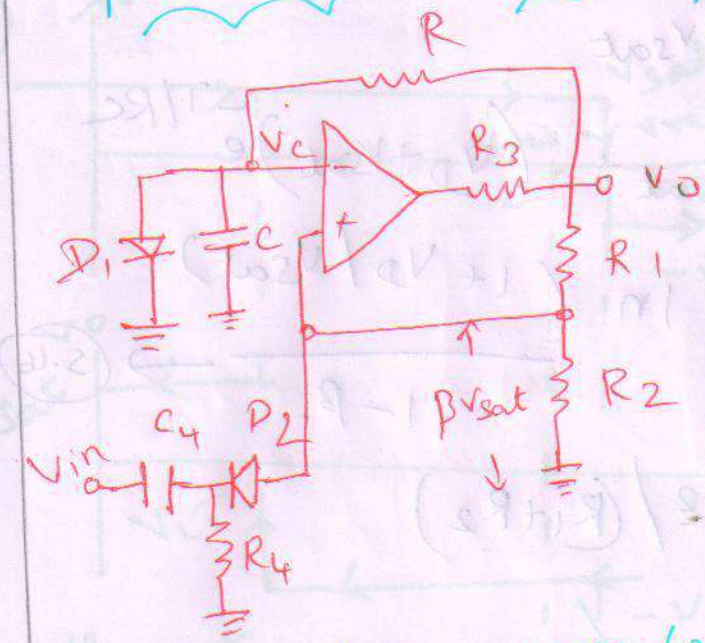
$$T = RC \ln \frac{1+\beta V_{o2}/V_{o1}}{1-\beta}$$

Monostable Multivibrator:-

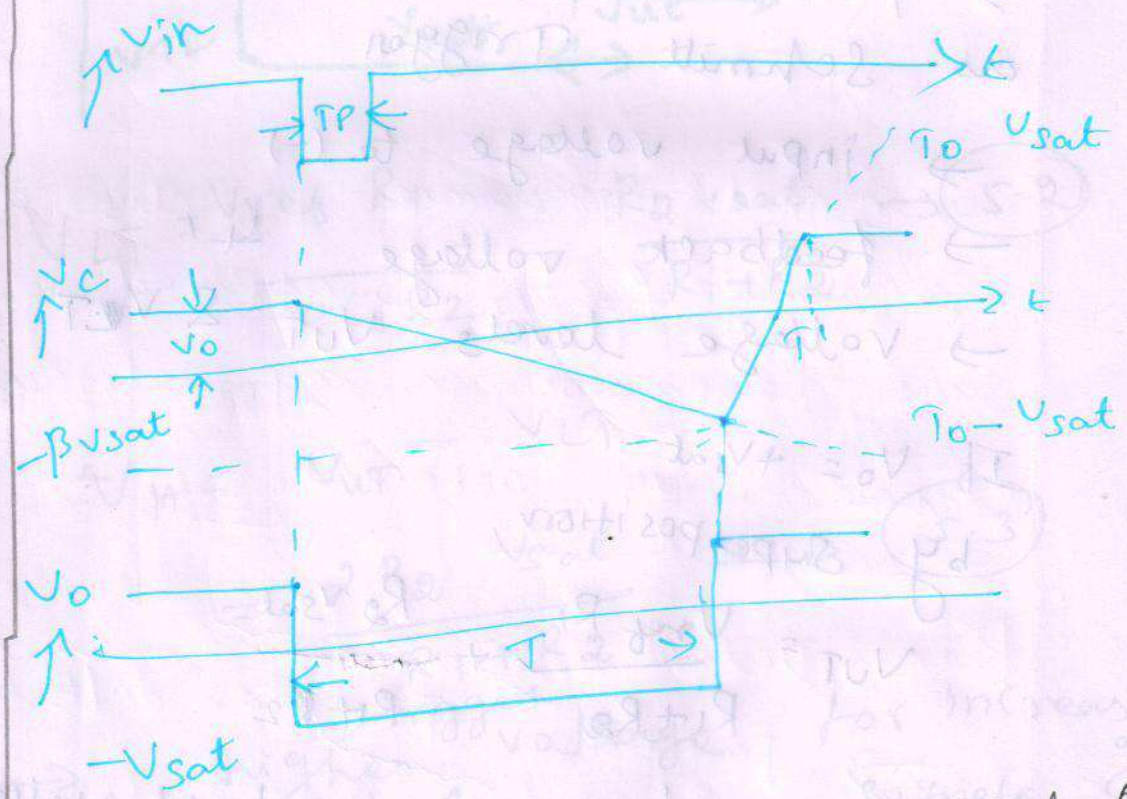
→ One Stable State to other is quasi Stable State.

→ Single o/p pulse of adjustable time duration.

Astable Multivibrator



o/p waveform



→ D_1 conducts (V_c is clamped to $+0.7V$)

$$V_o = V_f + (V_i - V_f)\, e^{-t/RC} \longrightarrow (5.13)$$

$$V_c = -V_{sat} + (V_D + V_{sat})\, e^{-t/RC} \longrightarrow (5.14)$$

$$V_C = -\beta V_{sat}$$

$$-\beta V_{sat} = -V_{sat} + (V_D + V_{sat}) e^{-T/RC}$$

$$T = RC \ln \left(\frac{1 + V_D / V_{sat}}{1 - \beta} \right) \rightarrow (5.16)$$

$$\beta = R_2 / (R_1 + R_2)$$

Wave form Generators :-

→ This circuit is also known as Schmitt Trigger

→ input voltage to (-)

→ feedback voltage '+'

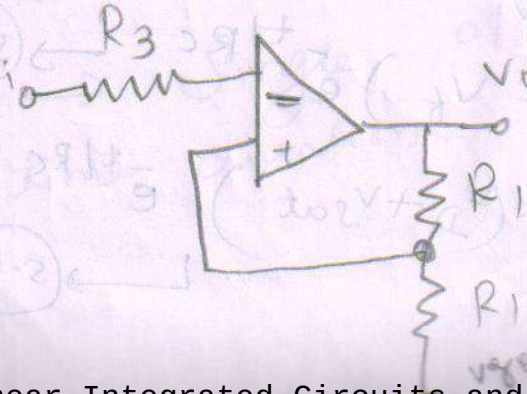
→ voltage levels V_{UT} & V_{LT}

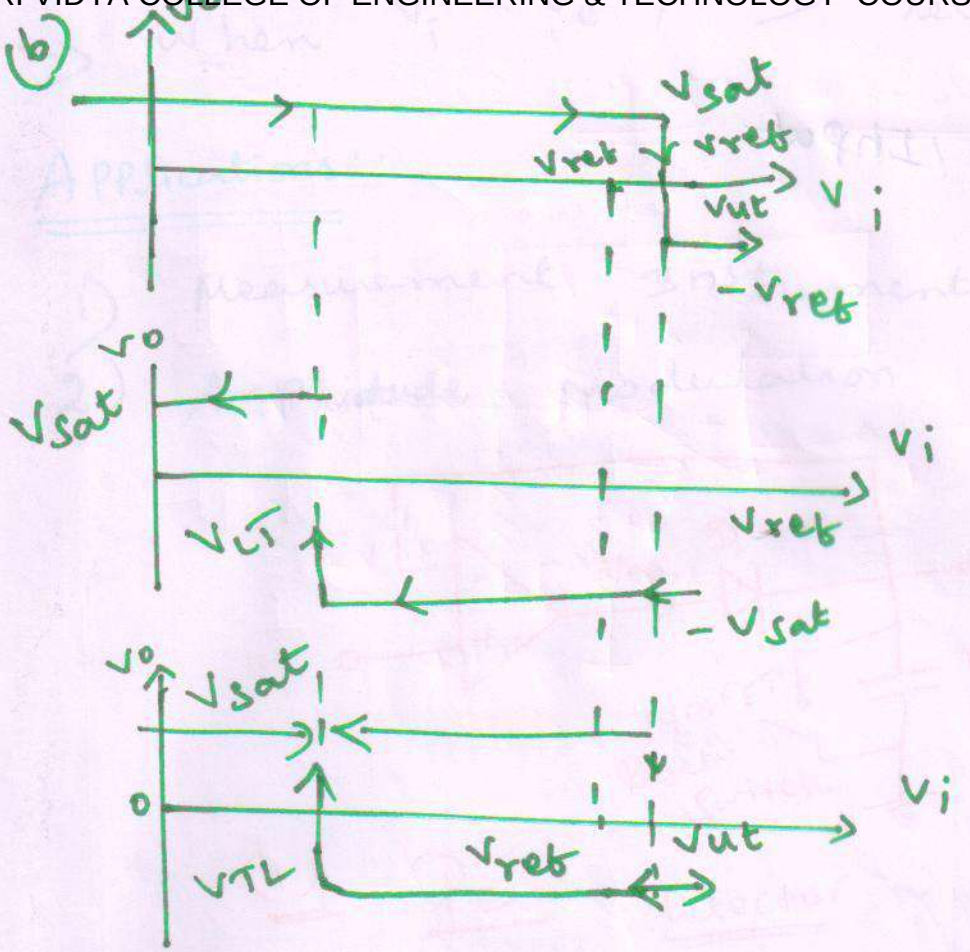
If $V_o = +V_{sat}$

by Superposition

$$V_{UT} = \frac{V_{ref} R_1}{R_1 + R_2} + \frac{R_2 V_{sat}}{R_1 + R_2}$$

V_{LT} ⇒ Lower threshold voltage





$$V_{LT} = \frac{V_{ref} R_1}{R_1 + R_2} - \frac{R_2 V_{sat}}{R_1 + R_2} \rightarrow (5.2)$$

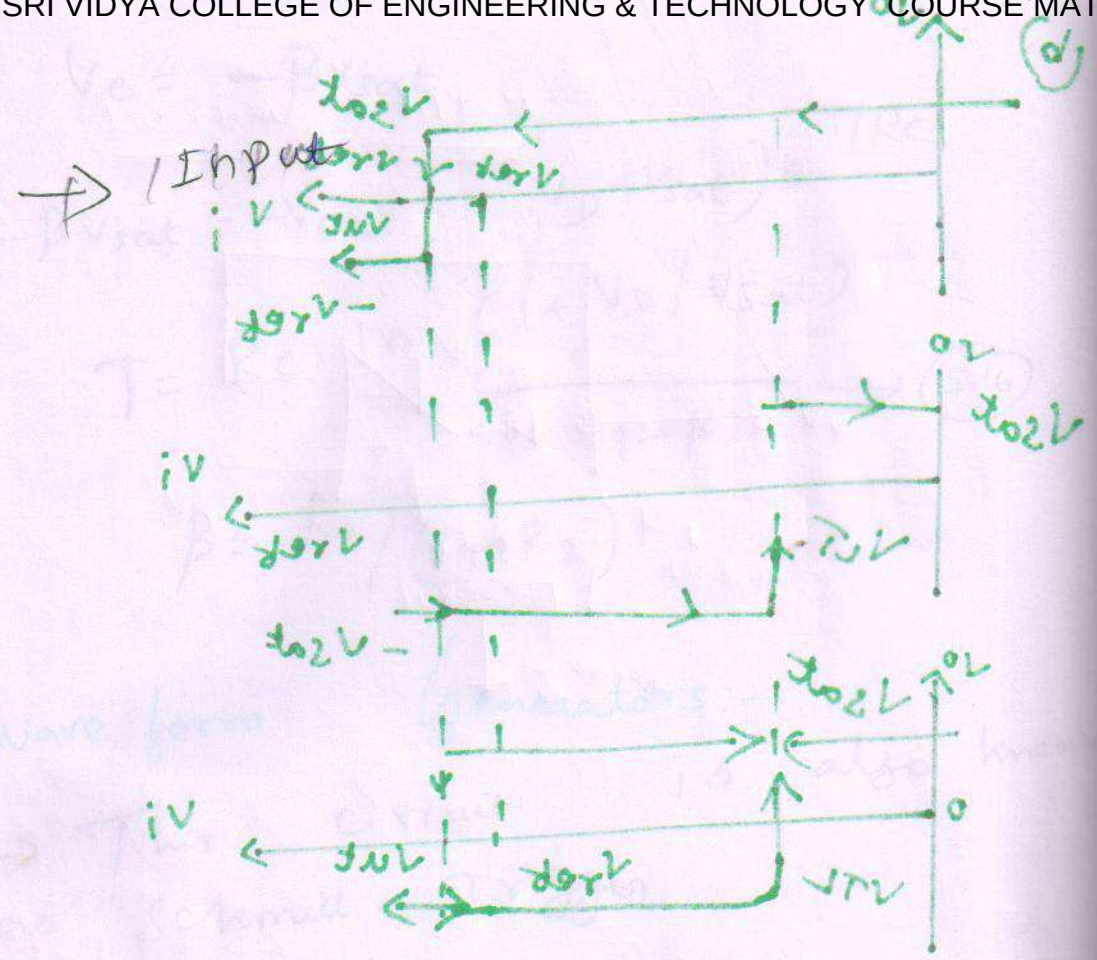
$$V_H = V_{UT} - V_{LT}$$

$$= \frac{2 R_2 V_{sat}}{R_1 + R_2} \rightarrow (5.3)$$

→ higher trigger voltage for increasing signals

→ input signal V_i is smaller than V_H

$$V_{UT} = -V_{LT} = \frac{R_2 V_{sat}}{R_1 + R_2}$$



→ Input impedance of sinusoid frequency $f = 1/T$ is applied to such comparator, a symmetrical square wave obtained.

Peak Detector :-

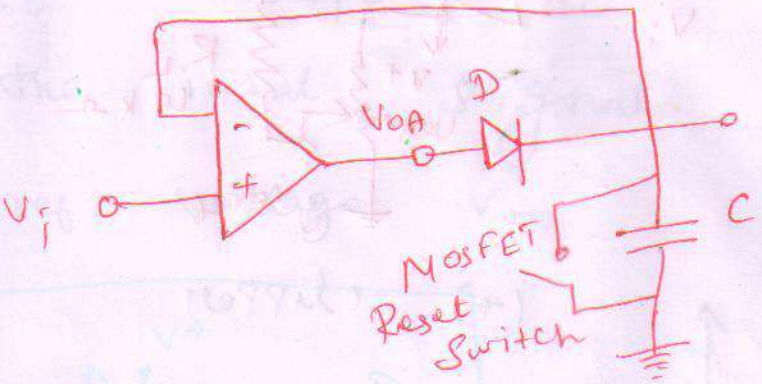
→ Function of Peak detector is to compute Peak value of input.

→ $V_i > V_c$ the Diode D is forward biased, the circuit becomes a voltage follower.

→ When V_i < V_{ref}, D reverse biased.

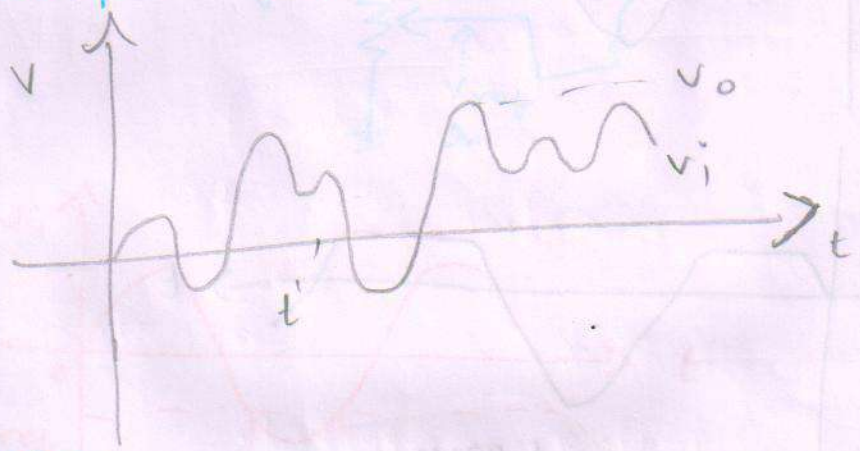
Applications:

1) Measurement Instrument
2) Amplitude Modulation



(+) Peak detector

output wave form

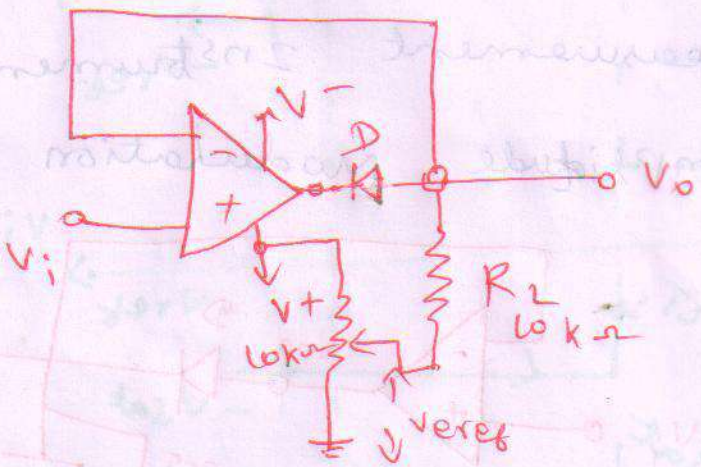


Clipper

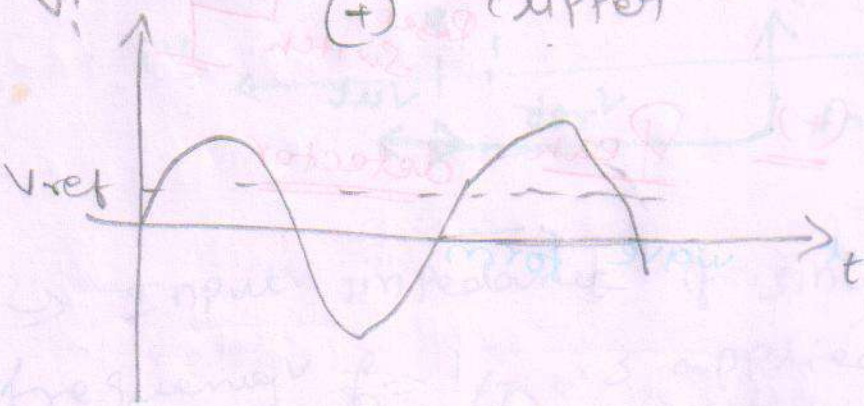
→ Used to Clip-off a Certain Portion of the input signal.

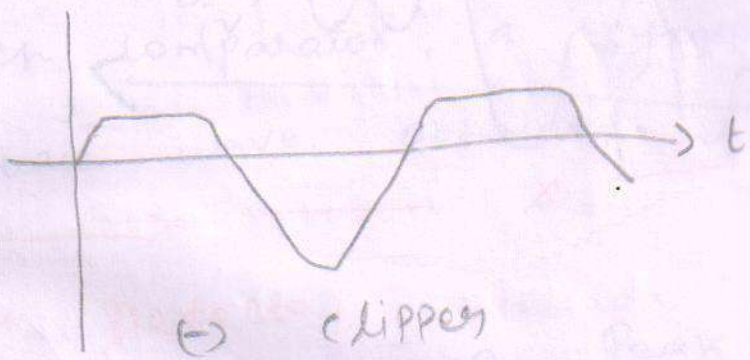
→ Clipping level is determined by Vref & Positive voltage V+

Positive clipper

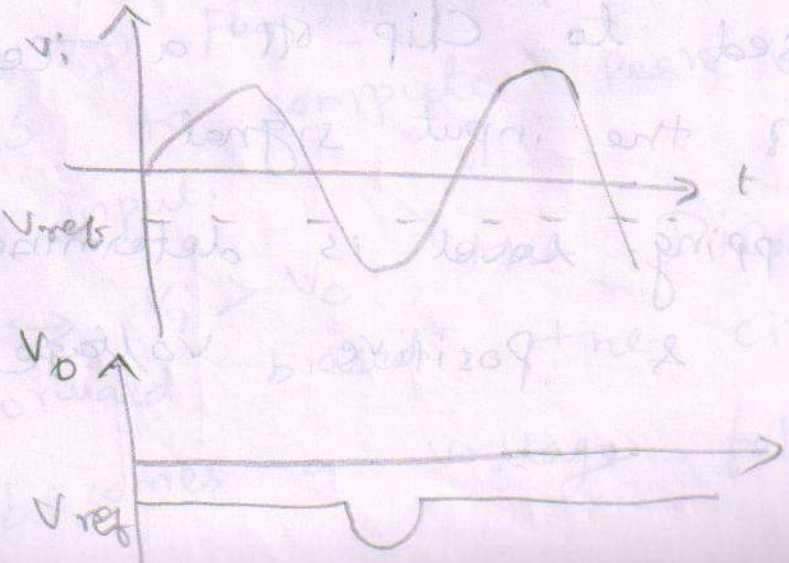


(+) clipper





(-) clipper

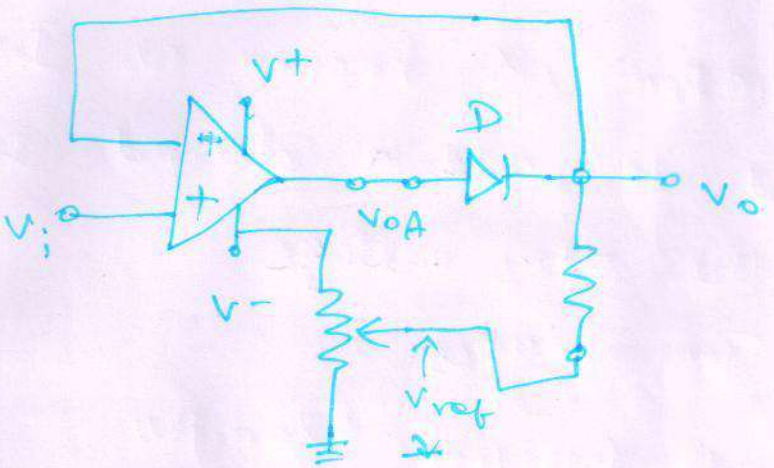


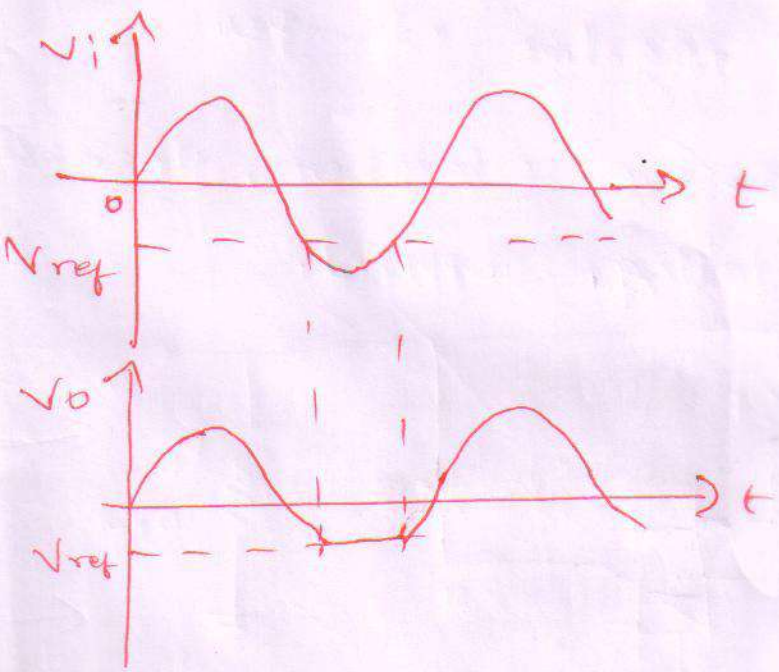
Negative Clipper :-

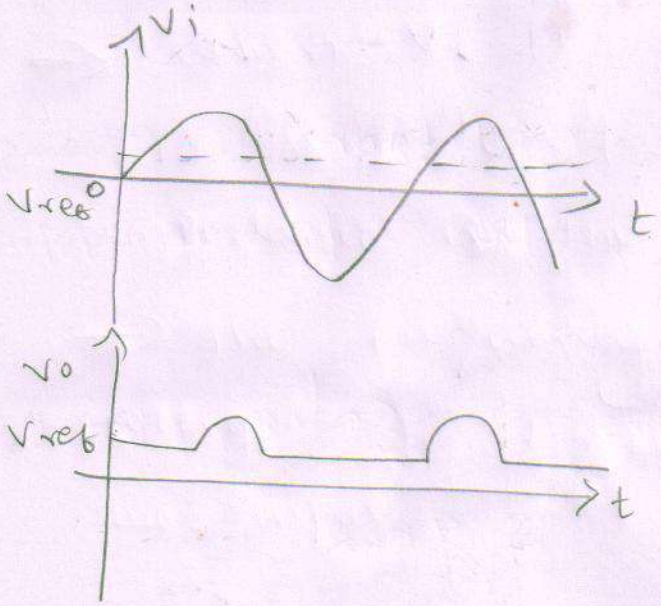
→ D reverse condition ie, Changing the Polarity of the reference voltage Vref.

→ It clips negative parts of the input signal

→ ref voltage Vref.







Clamper :-

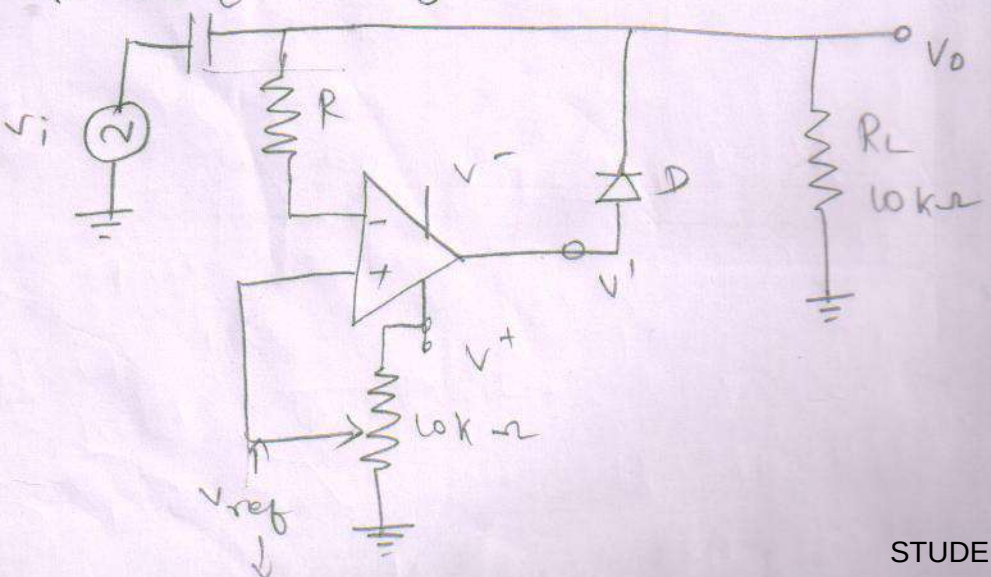
→ Clamper is known as Dc inserter

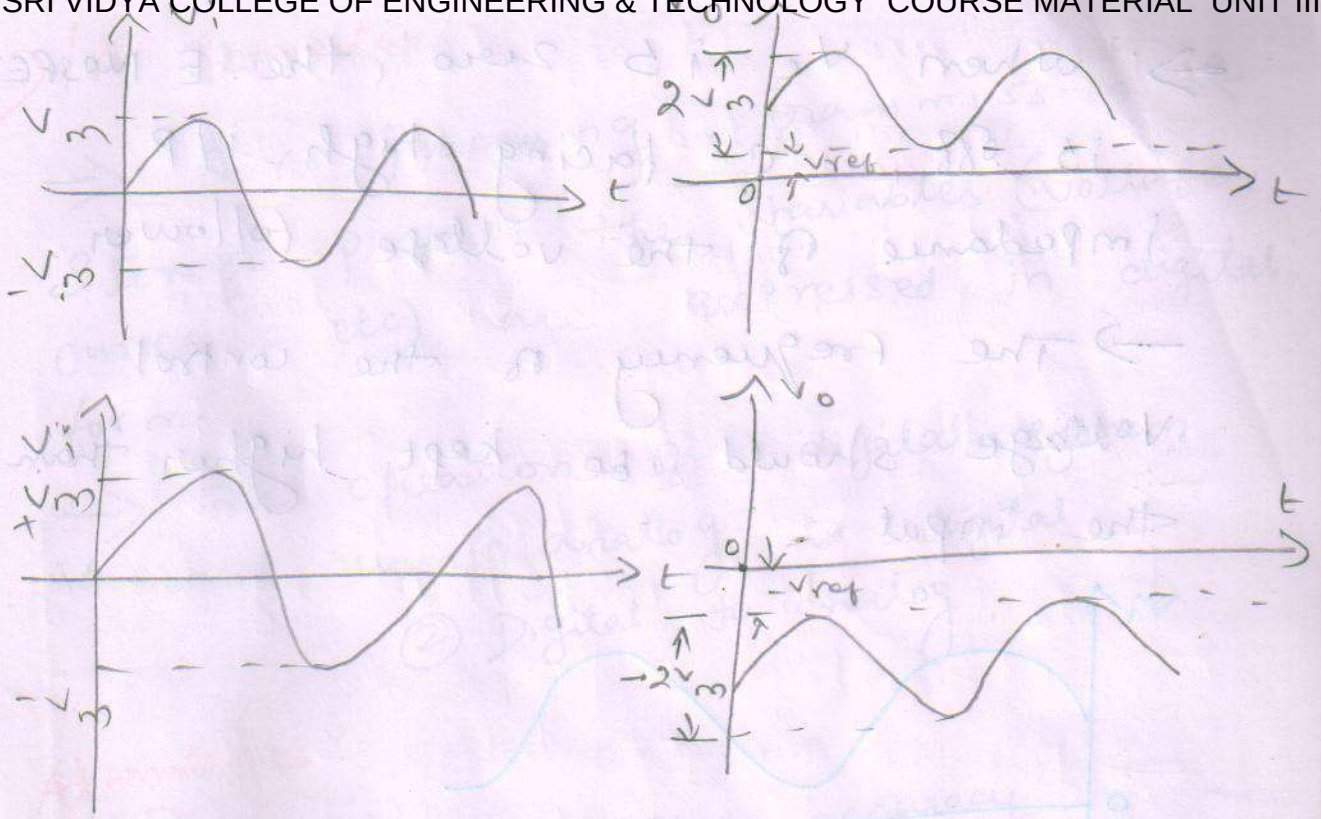
→ used to add a desired Dc level to the o/p voltage

Two types

1) Positive clamper
2) negative clamper

→ In Positive clamper, variable '+' ve Dc voltage applied.

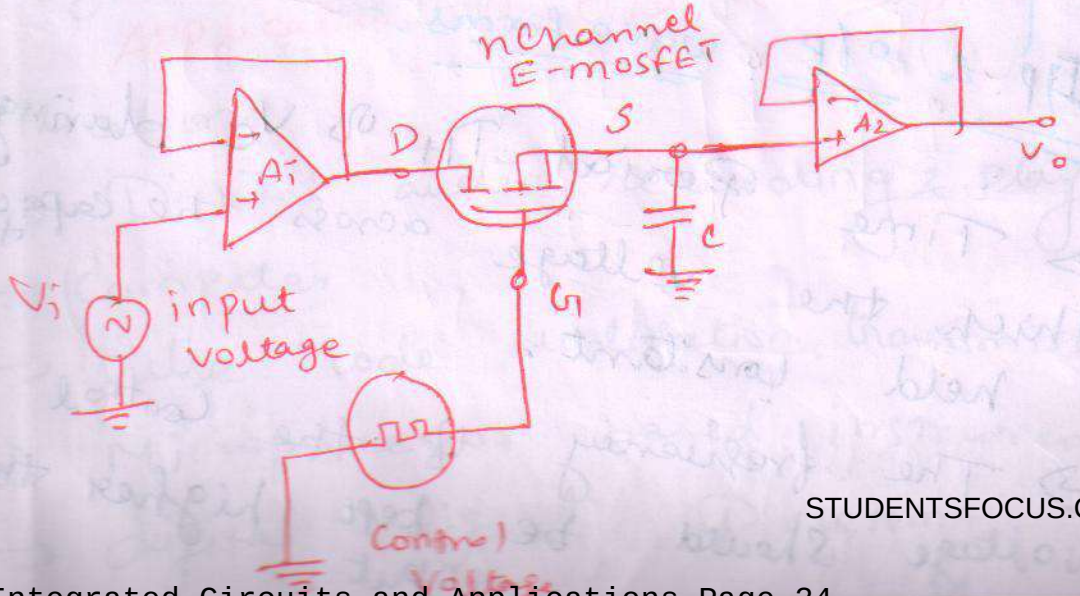




Sample and Hold circuit :-

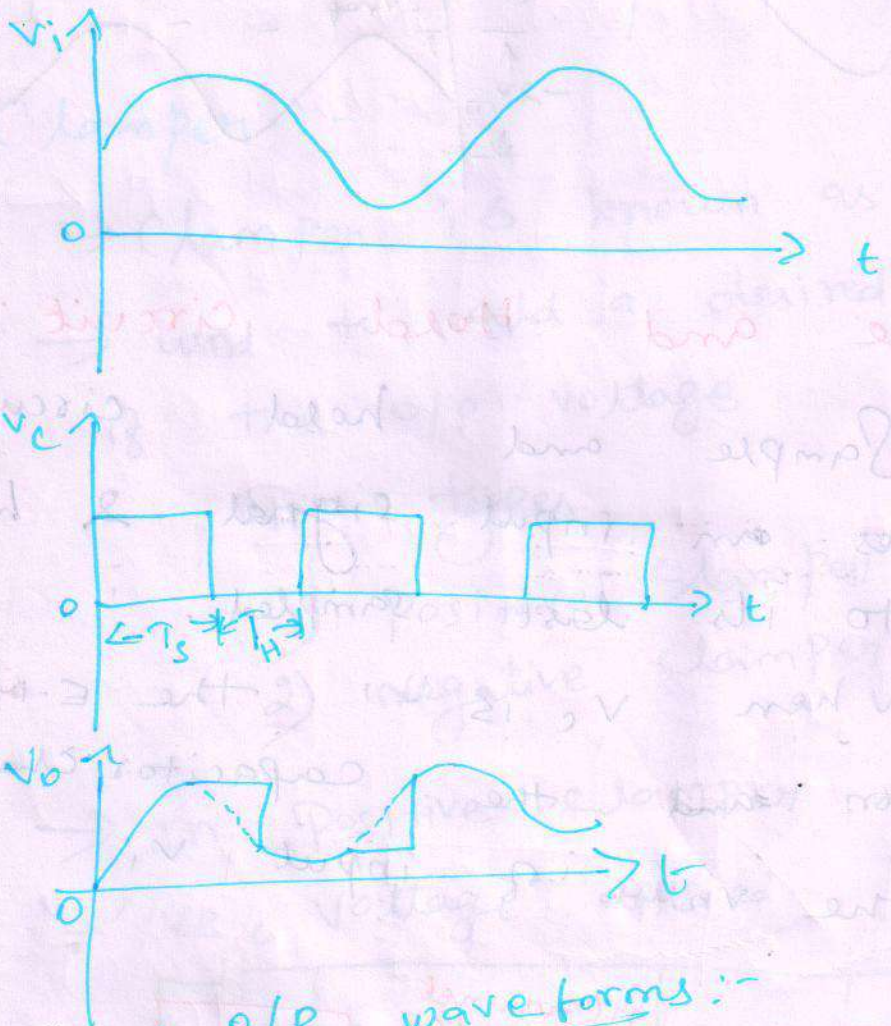
→ Sample and hold circuit Samples an input signal & holds on to its last sampled.

→ when V_c is '+' the E-MOSFET turns on and the capacitor charges to the value of input V_i



→ When V_c is zero, the E MOSFET is off, C facing high i/p impedance of the voltage follower.

→ The frequency of the control voltage should be kept higher than the input



I/p & o/p waveforms :-

→ Time Period T_H of V_c during which the voltage across the capacitor is held constant.

→ The frequency of the control voltage should be kept higher than input

D/A Converter:-

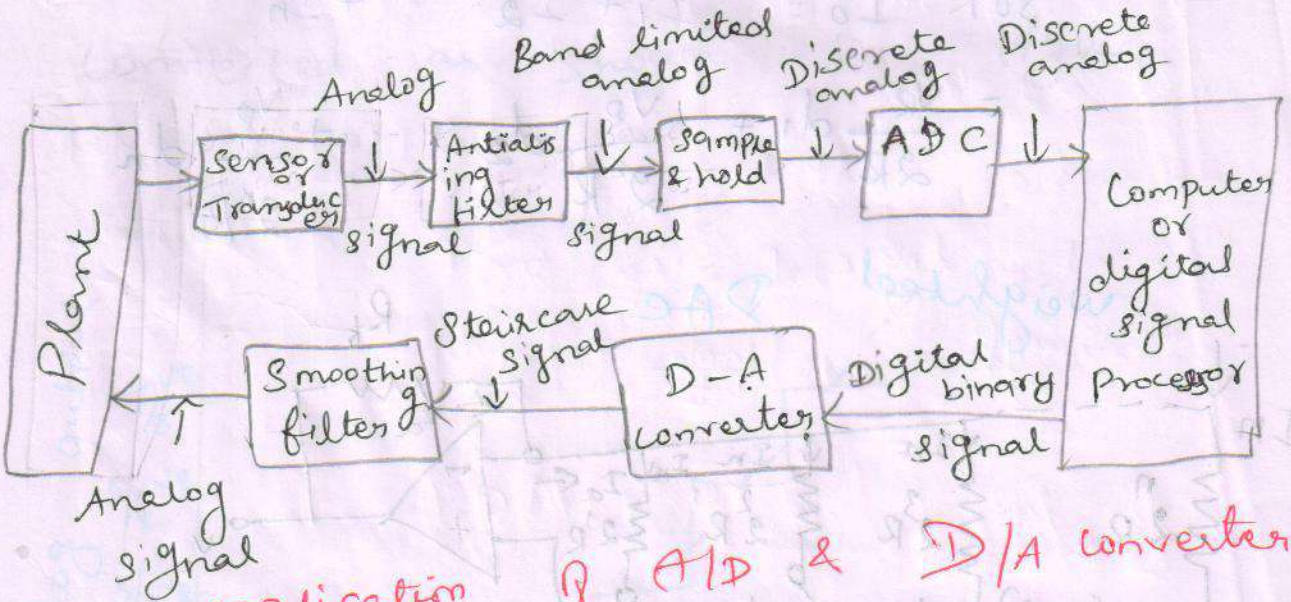
→ for Processing, transmission & Storage purpose the variables (voltage, current etc) are expressed in digital form.

→ The operation of digital system is based upon ① analog to digital ② Digital to analog.

Advantages:-

→ It gives better accuracy

→ It reduces noise



Applicatin of A/D & D/A converter

Applications:-

→ Digital audio recording & playback

→ Computer

→ pulse code Modulation transmission

→ Microprocessor based instrumentation

→ digital Signal Processing

There are Three techniques,

1) weighted resistor DAC
2) R-2R ladder
3) Inverted R-2R ladder

Weighted Resistor :-

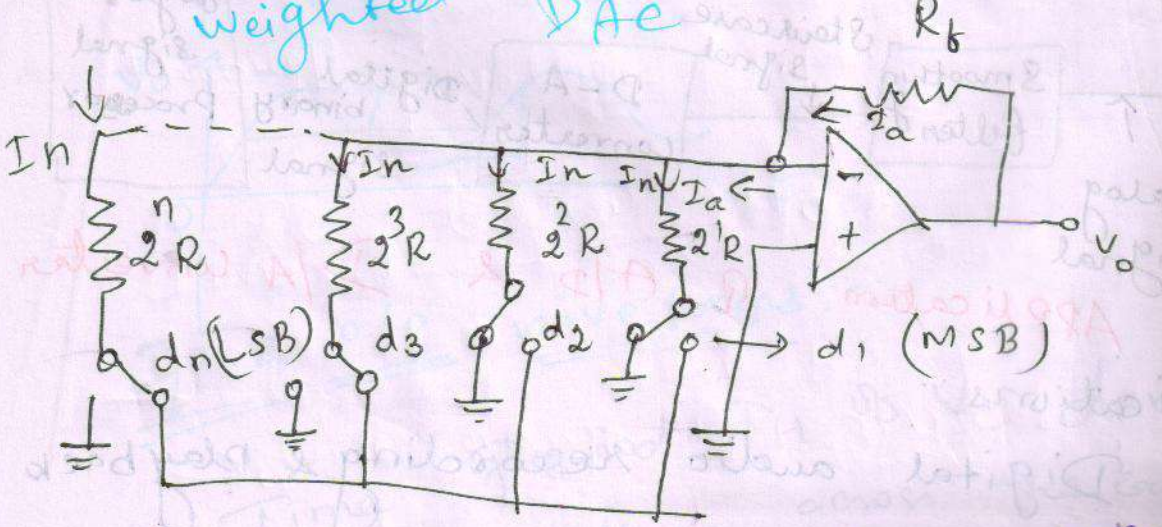
→ It has n electronic switches $d_1 d_2 \ldots d_n$ controlled by binary input word.

→ If the input bit is 0 the switch connects the resistor to the ground.

So, $I_0 = I_1 + I_2 \cdots + I_n$

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \cdots + \frac{V_R}{2^n R} d_n$$

weighted DAC



$$\Rightarrow \frac{V_R}{R}\left(d_1 2^{-1} + d_2^{2-2} + \cdots + d_n^{2-n}\right)$$

o/p voltage

$V_o = I_o R_f$

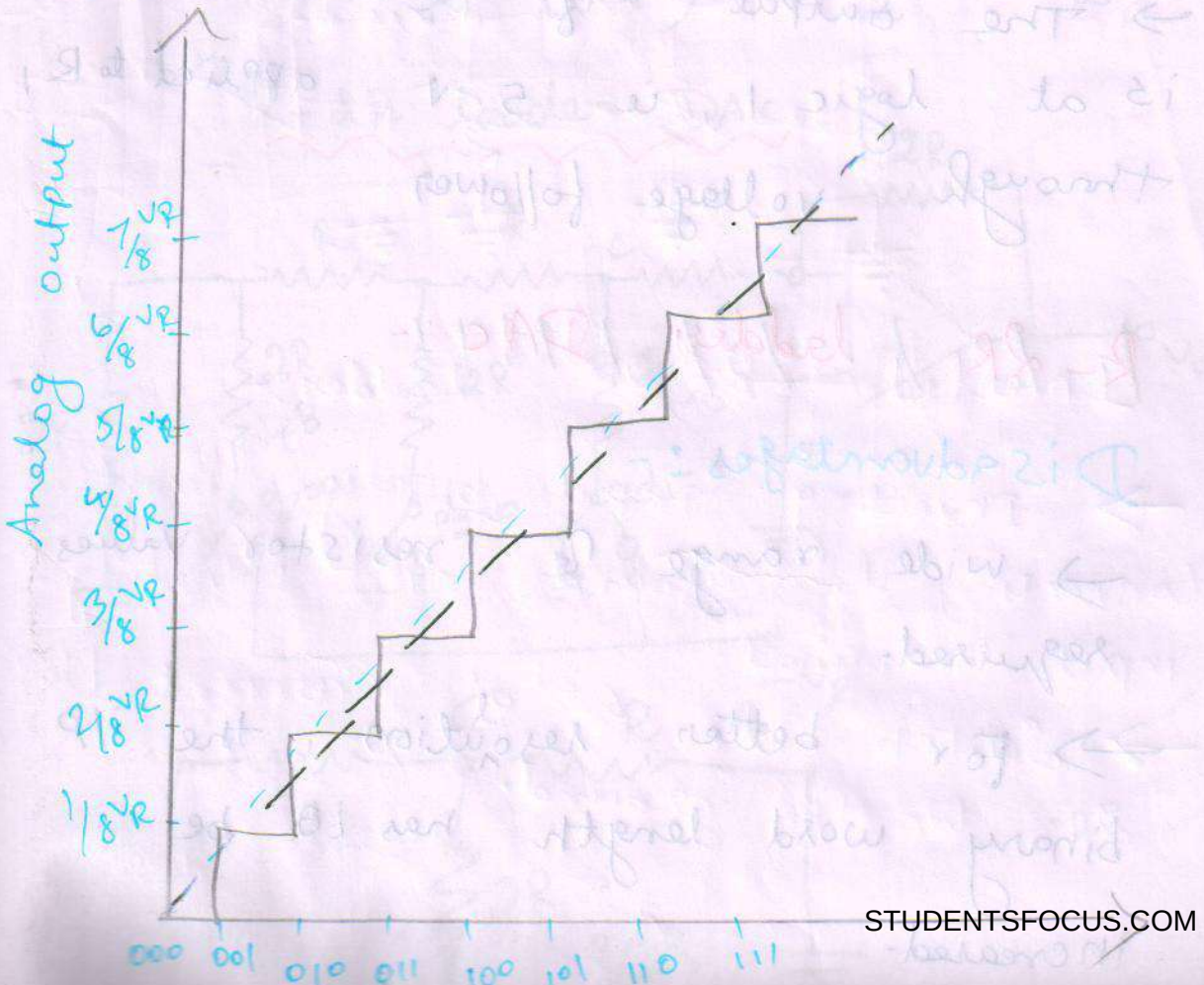
$= V_R \frac{R_f}{R} (d_{12} + d_2 2^{-2} + \dots + d_n 2^{-n})$

→ It working as a current to voltage Converter

→ Reference voltage should be +5V & o/p will be negative

→ On resistor must be very low & they should have zero Offset voltage.

→ Different types of digitally controlled SPDT electronic switches are available of which two are connected as shown in figure



→ two Complementary gate inputs Q & $\bar{Q}$ come from MOSFET S-R flipflop

→ logic '1' corresponds to -10V & logic '0' corresponds to zero volt.

→ If there is '1' in the bit line S=1 & R=0, Q=1 & $\bar{Q}$=0

→ This drives the transistor Q_2 on

→ $-V_R$ means transistor Q_2 remains off.

→ $\bar{Q}$=0 makes transistor Q_1 off & Q_2 on.

→ The output of CMOS inverter is at logic 1, ie 5 V applied to R_1 through voltage follower.

R-2R / ladder / DAC :-

Disadvantages :-

→ wide range of resistor values required.

→ For better resolution, the i/p binary word length has to be increased.

→ Number of bit increases, the range of resistance value increases.

R-2R Ladder DAC :-

→ wide range of resistors

→ Two values of resistor are required.

→ Switch Positions $d_1\ d_2\ d_3 \rightarrow$ 100

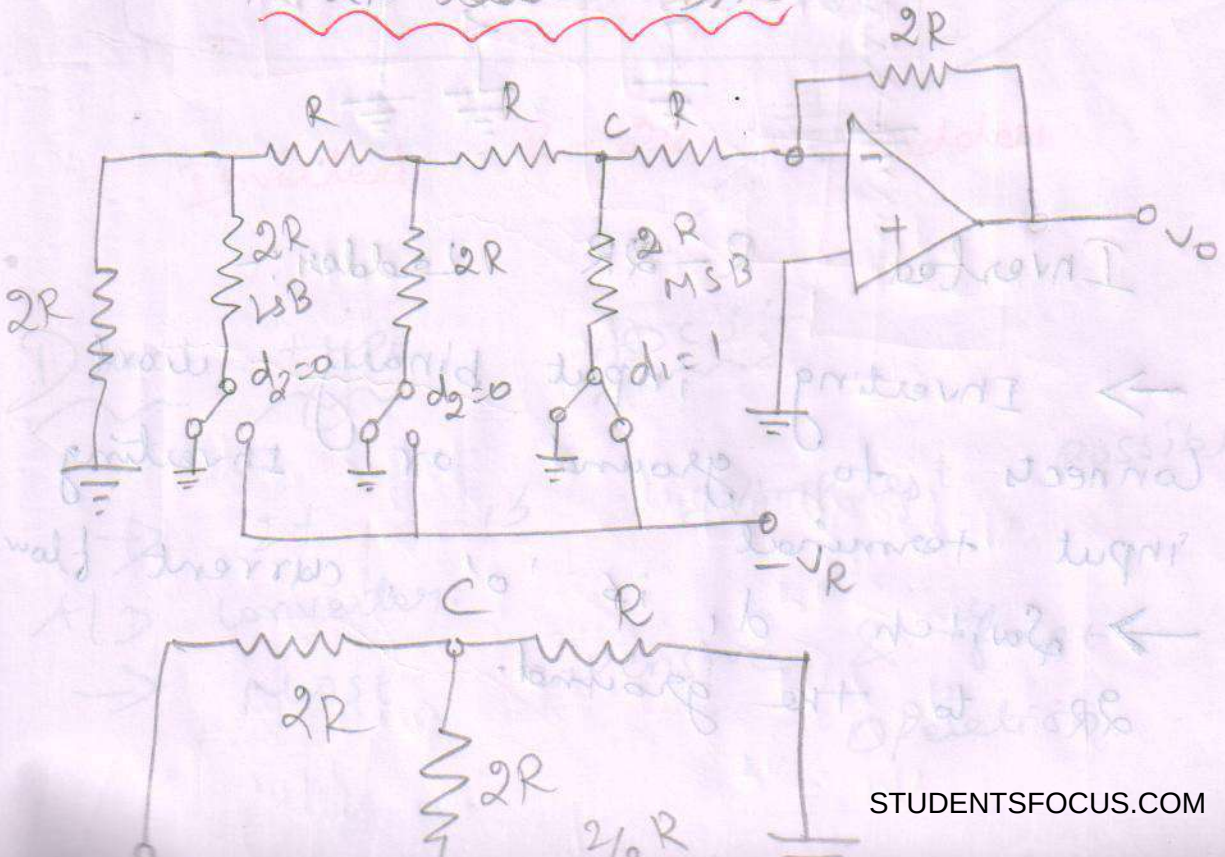
The voltage at node c is

$$\frac{-V_R\left(\frac{2}{3}R\right)}{2R+\frac{2}{3}R} = \frac{-V_R}{4}$$

The output voltage is

$$V_o = \frac{-2R}{R}\left(\frac{-V_R}{4}\right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$$

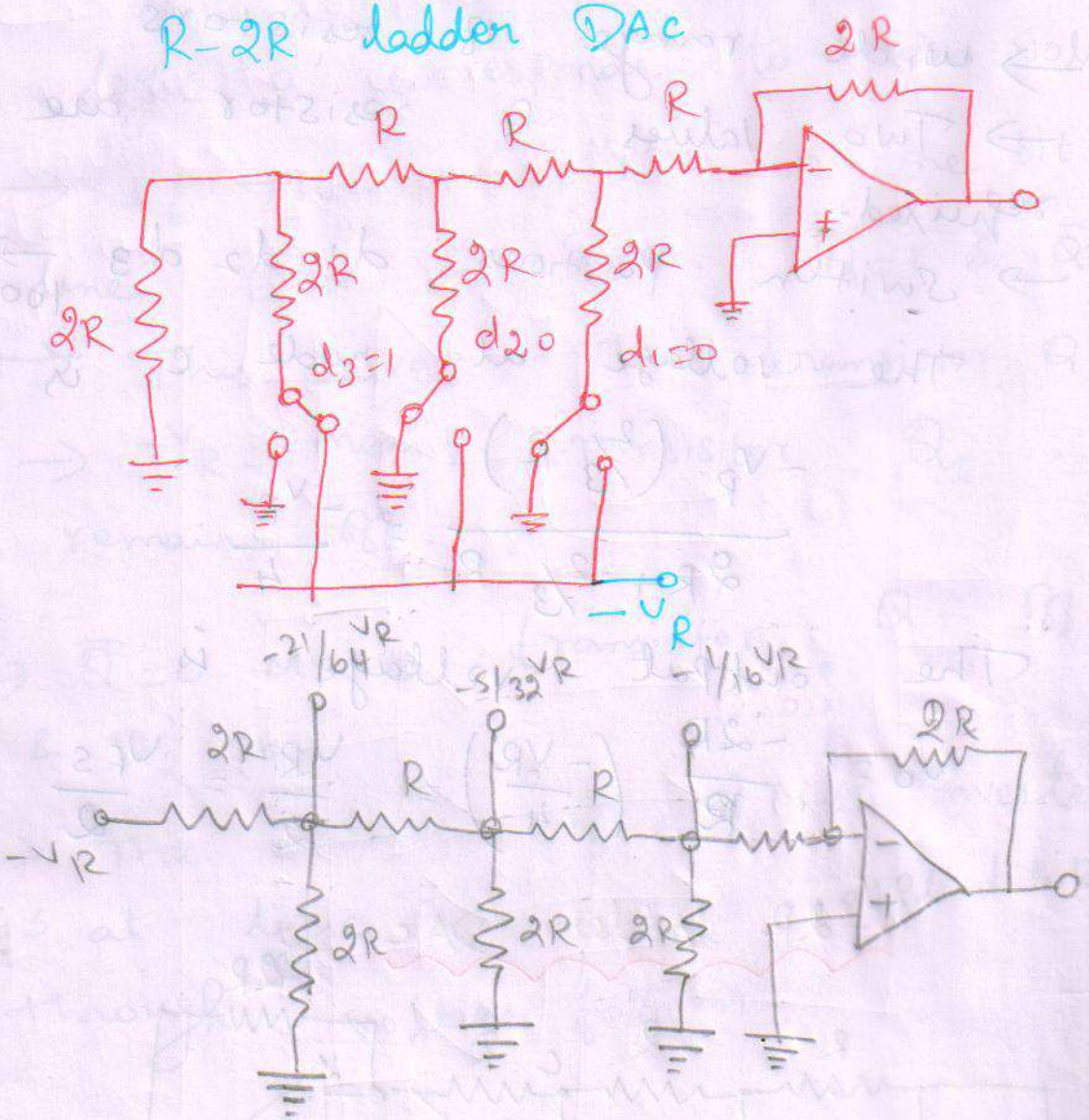
R-2R ladder DAC



The o/p voltages becomes,

$$V_o = \left(-\frac{2R}{R}\right)\left(\frac{-V_R}{16}\right) = \frac{V_R}{8} = \frac{V_{FS}}{8}$$

R-2R ladder DAC



Inverted R-2R Ladder :-

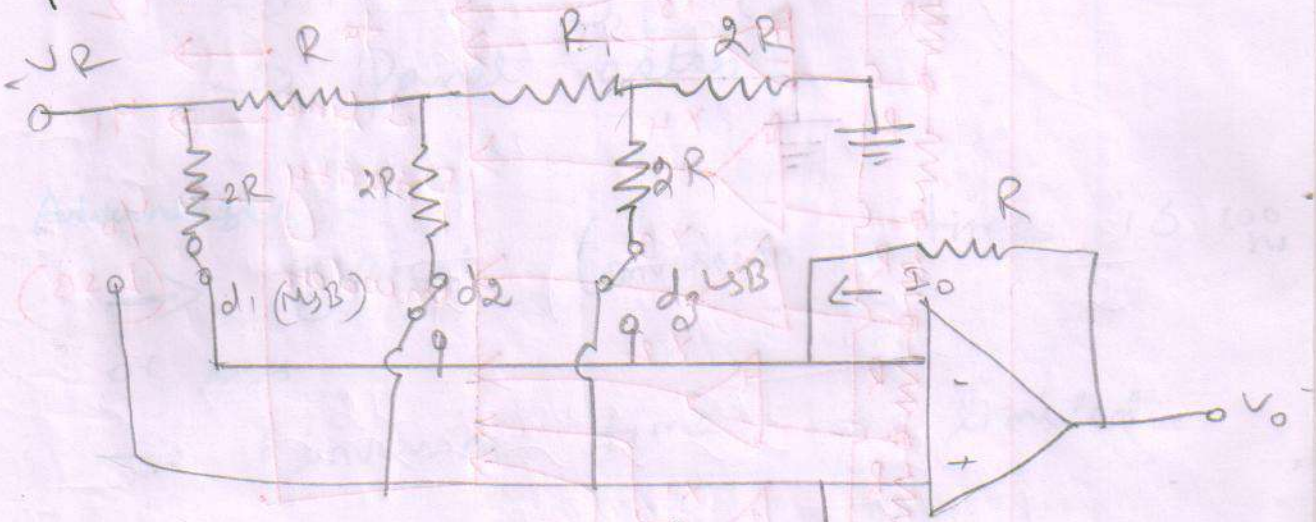
→ Inverting input binary word Connects to ground or Inverting input terminal

→ Switch d_1 is '0', current flowing 2R to the ground.

→ When d_i is at logical 1, the current through 2R sinks to the virtual ground.

→ current remains constant in each branch of ladder

→ The current flows from inverting i/p terminal to $-V_R$ for $d_i = 1$, & from ground to $-V_R$ for $d_i = 0$.



Inverted R–2R ladder

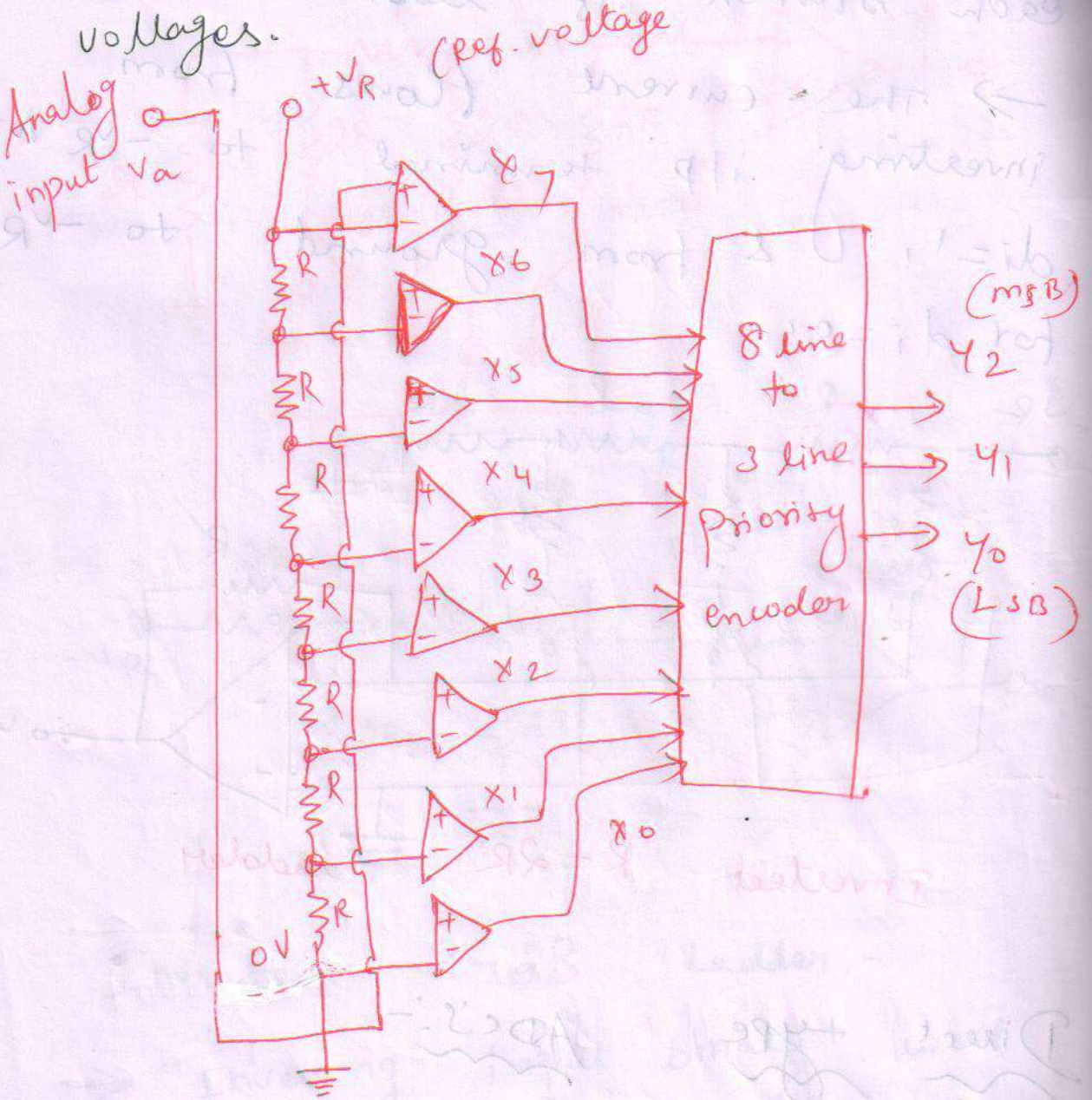
Direct type ADC's:-

→ It is Simplest possible A/D converter.

→ Most expensive & fast Operation.

→ Consists of a resistive divider network & op-amp, 8 line to 3 line encoder.

→ to compare the analog voltage Va with each of the node voltages.



voltage input	logic output
$V_a \geq V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	previous value

Comparator

Applications :-

→ data loggers
→ Instrumentation where conversion is important
Speed
→ digital meter
→ Monitoring systems
→ Panel meter

Advantages :-

→ typical Conversion time is 100 ns or less
→ Conversion time is limited

Disadvantages :-

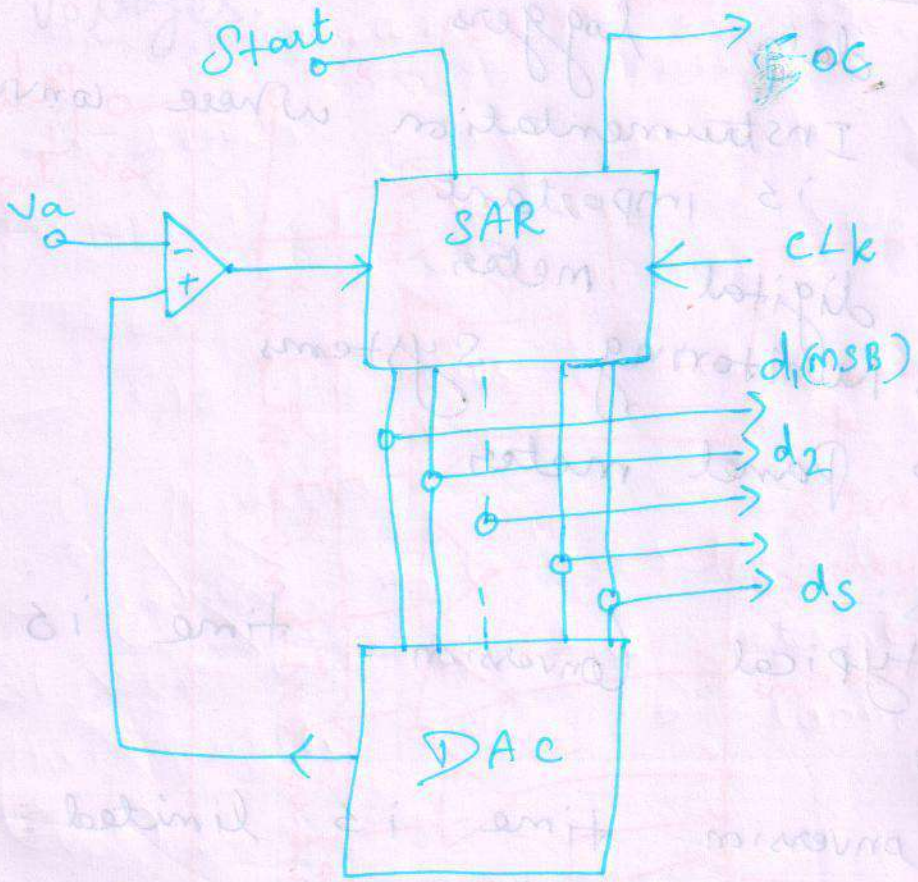
→ the number of Comparators required almost doubles for each bit.
→ More Complex

Successive Approximation Converter

→ Eight bit Converter require 8 clock Pulse to obtain a digital o/p

→ SAR required value of each bit by trial & error.

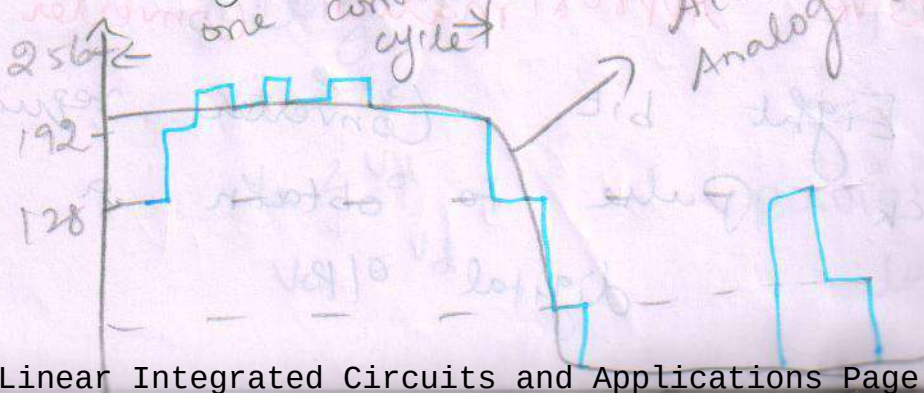
→ Sets the MSB $d_1 = 1$ with all other bits '0', trial code is 10000000



Functional Diagram

→ If Va > DAC o/p V_d then 10000000 is less.

→ If Va < DAC o/p the 10000000 is greater.



⇒ Reset MSB to 0 & go on to the next lower Significant bit

Correct digital Representation	SAR O/P V_d	Comparator O/P
11010100	10000000	1
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

Integrating type of ADC's

⇒ Do not require a S/H circuit at the input

⇒ Input Changes, ADC O/P Code will be a value of input averaged over the integration period.

Charge balancing ADC :-

⇒ Covert input signal to a frequency

⇒ output code is to analog input

⇒ output V/F Converter depends upon an RC Product

Drawback :-

Charge balancing ADC is eliminated

Dual Slope ADC

→ Consists of high input impedance buffer A_1, Precision integrator A_2 & voltage comparator.

→ V_R is opposity Polarity until the integrator o/p is zero.

→ START, the switch SW_1 is connected to ground, SW_2 is close.

→ C_{A2} Provides Automatic Compensation.

→ Counter resets itself to zero at the end of the interval T_1 & the switch SW_1 is connected to $(-V_R)$.

Analog input voltage V_a then

$$T_1 = t_2 - t_1 = \frac{2^n \text{ counts}}{\text{clock rate}}$$

$$t_3 - t_2 = \frac{\text{digital count } N}{\text{clock rate}}$$

Integrator

$$\Delta V_o = (-1/RC)\, V \Delta t$$

$$V_1 = (-1/RC)\, V_a (t_2 - t_1)$$

$V_1 = \left(-\frac{1}{RC}\right)(-V_R)(t_2 - t_1)$

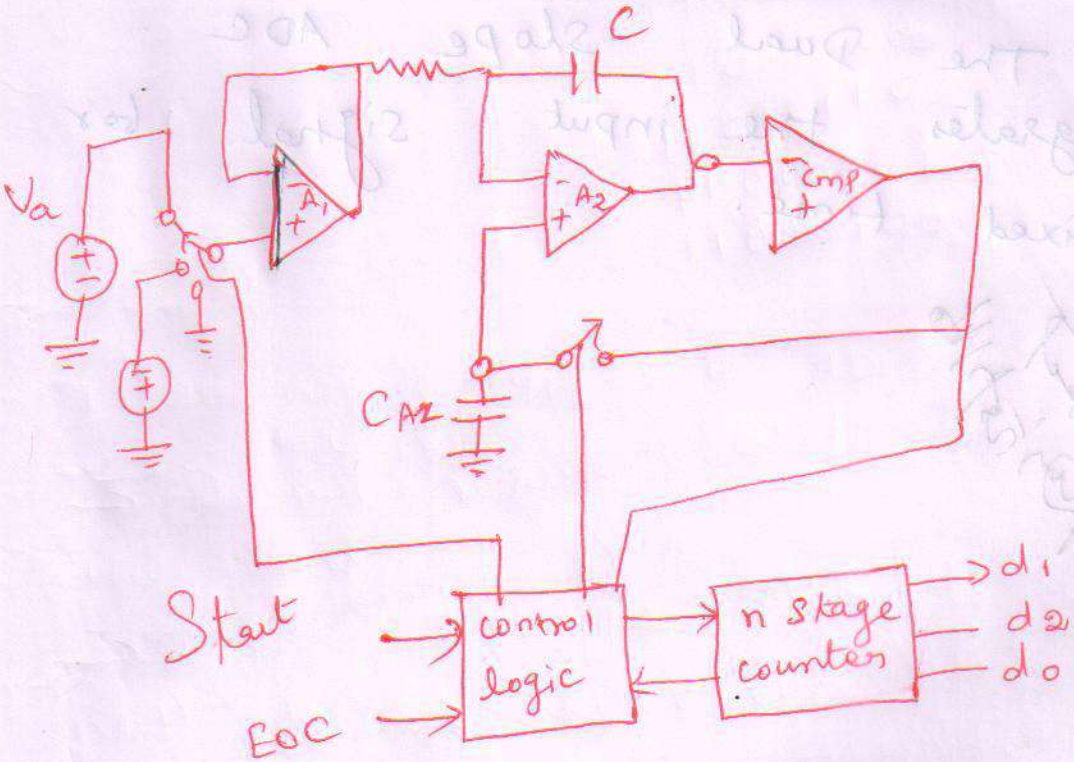
$= V_a (t_2 - t_1) = V_R (t_3 - t_2)$

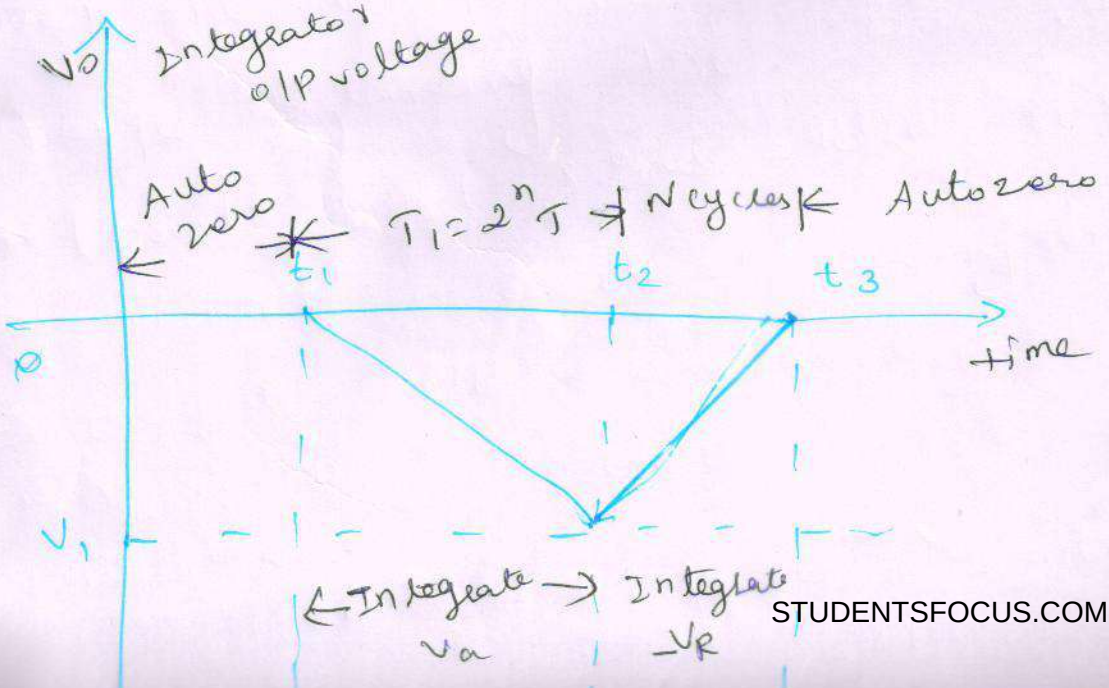
Putting the values of $t_2 - t_1 = 2^n$

& $t_3 - t_2 = N$

$V_a (2^n) = (V_R) N$

$V_a = (V_R)(N/2^n)$





Important Observations :-

→ V_R & n constant, $V_a \propto N$ and independent of R, C & T

→ $\log_2^n$ Conversion time

→ It is applicable for slowly varing signals ie weighing scales & thermo couples.

→ The Dual slope ADC integrates the input signal for a fixed time.

Cost is Comparatively High

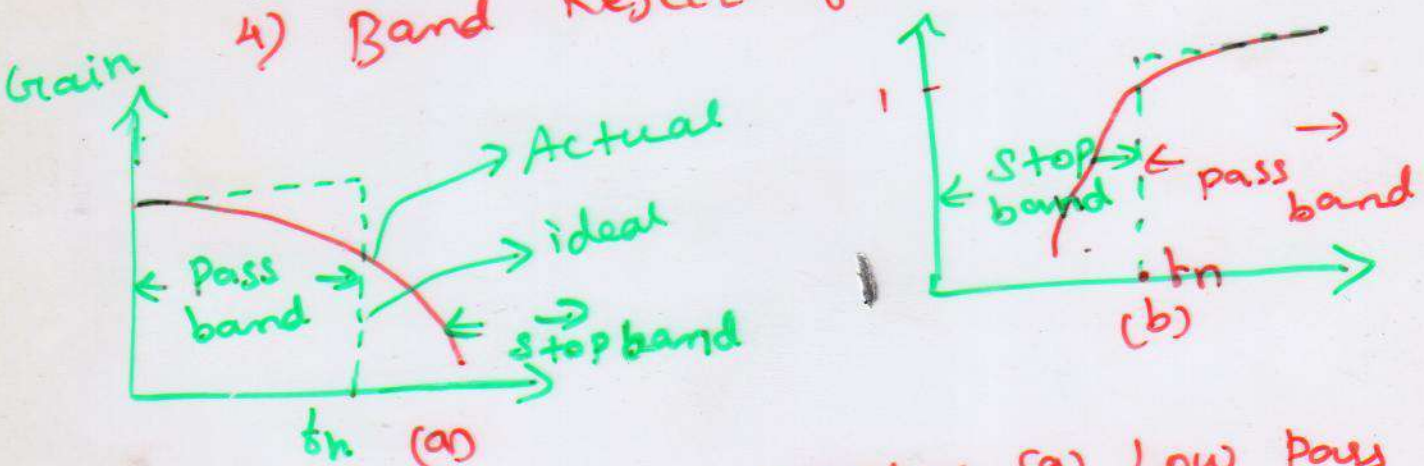
Active Filters

→ Filters are used in communication & signal processing and all electronic instruments.

→ They use op-amp as the active elements. & resistors and capacitors as the passive elements.

The most commonly used filters are

1) Low pass filter
2) High pass filter
3) Band pass filter
4) Band Reject filter



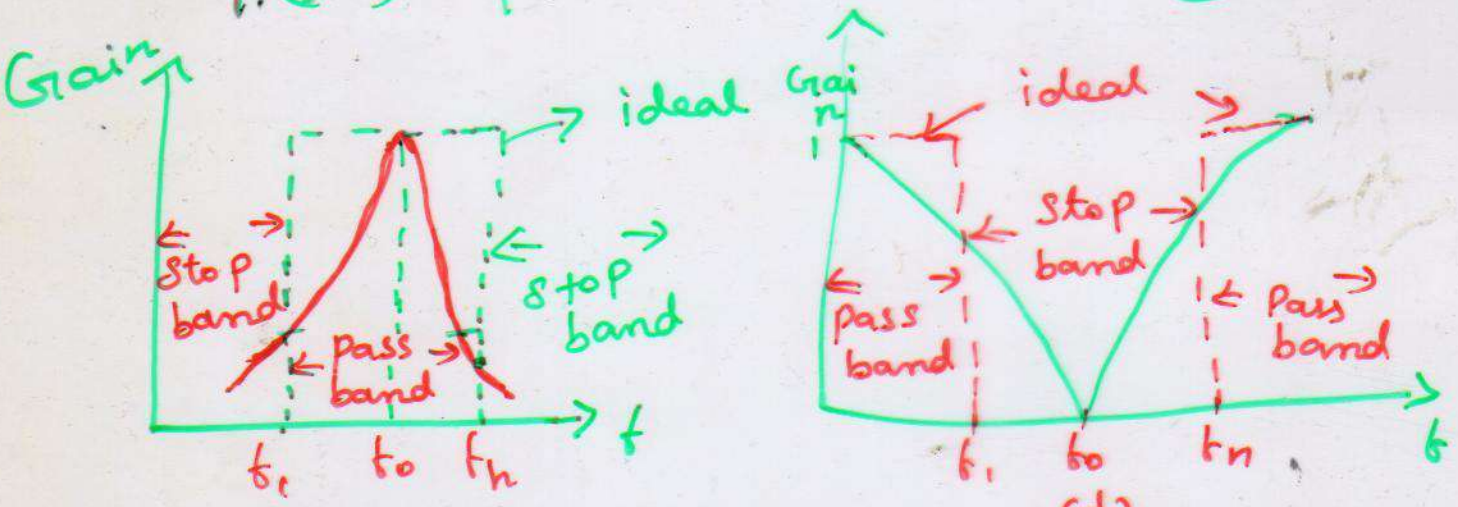
Frequency response of filters (a) Low pass (b) high pass filters.

Transfer function

$$H(s) = \frac{V_0(s)}{V_i(s)}$$

Under Steady State condition,

$$H(j\omega) = |H(j\omega)| e^{j\phi(\omega)} \quad \text{——— (7.1)}$$

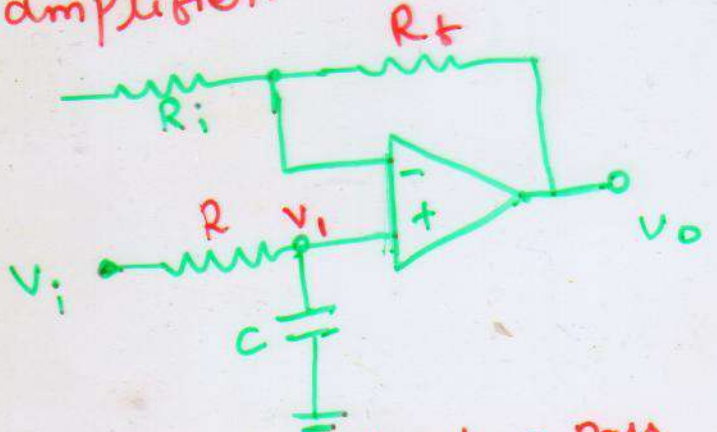


(c) (d)

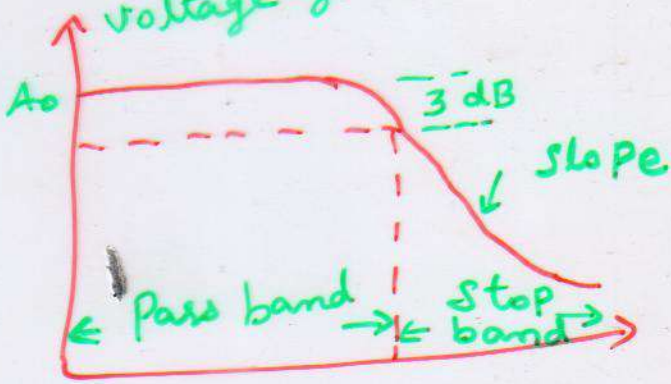
Frequency response of filters (c) Band pass (d) Band-reject.

First order low pass filter :-

→ Consists of single Rc network connected to the inverting and non inverting amplifier.



First order low pass filter



Frequency Response

The voltage across the capacitor

$$C_1 \rightarrow V_1(s) = \frac{1/sC}{R + 1/sC} V_i(s)$$

$$\frac{V_1(s)}{V_i(s)} = \frac{1}{RCs+1} \rightarrow (7.4)$$

Closed loop gain,

$$A_o = \frac{V_o(s)}{V_1(s)} = 1 + \frac{R_F}{R_i} \rightarrow (7.5)$$

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{V_o(s)}{V_1(s)} \cdot \frac{V_1(s)}{V_i(s)} = \frac{A_o}{RCs+1} \rightarrow (7.6)$$

$$\omega_h = 1/RC \rightarrow (7.7)$$

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{A_o}{s/\omega_h + 1} = \frac{A_o\omega_h}{s+\omega_h} \rightarrow (7.8)$$

$$H(j\omega) = \frac{A_o}{1+j\omega RC} = \frac{A_o}{1+j\omega RC} = \frac{1}{1+j(f/f_h)} \rightarrow (7.9)$$

$$f_h = \frac{1}{2\pi RC} \quad \& \quad f = \frac{\omega}{2\pi}$$

very frequency $f << f_h$

$$|H(j\omega)| = A_o$$

$f = f_h$

$|H(j\omega)| << A_o \approx 0$, if $f >> f_h$

→ Frequency range from 0 to f_h

→ pass band.

→ $f > f_h$ stop band

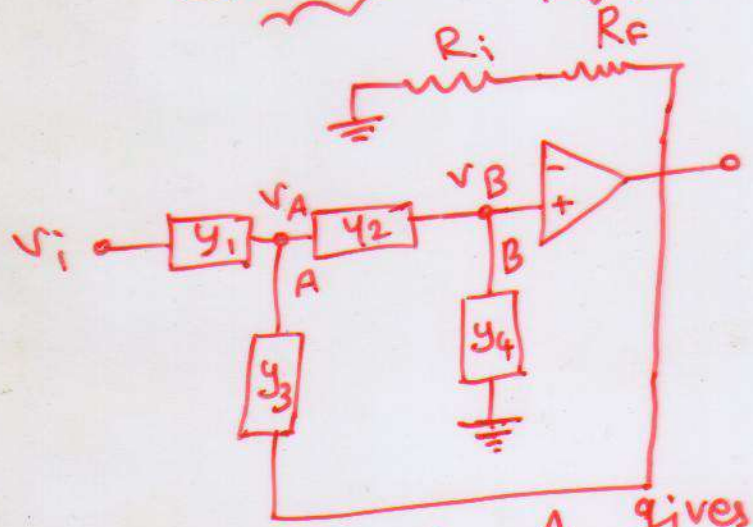
Second Order Active Filter :-

An improved filter response can be obtained by using second order Active filters.

$$V_o = \left(1 + \frac{R_F}{R_i}\right) V_B = A_o V_B \quad \rightarrow (7.13)$$

$$A_o = 1 + \frac{R_F}{R_i} \quad \rightarrow (7.14)$$

Circuit Diagram



KCL law, at A gives

$$V_i Y_1 = V_A(Y_1+Y_2+Y_3) - V_o Y_3 - V_B Y_2$$

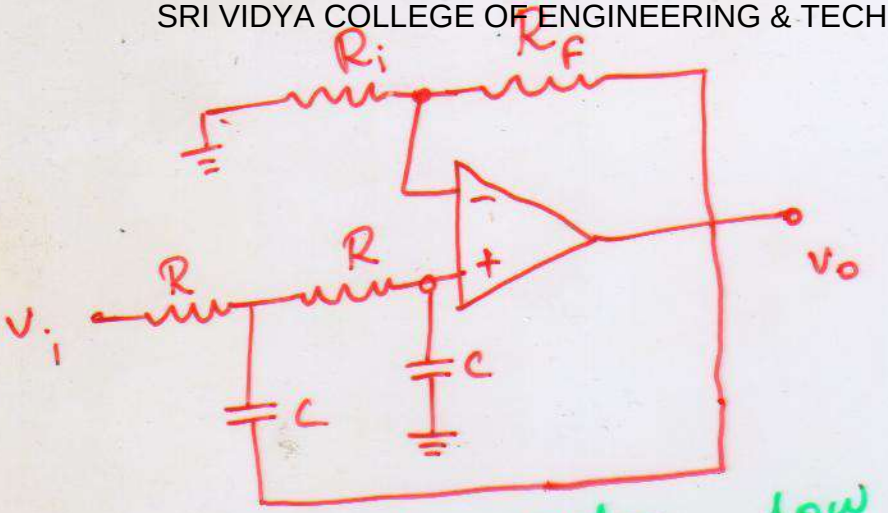
$$= V_A (Y_1+Y_2+Y_3) - V_o Y_3 - \frac{V_o Y_2}{A_o} \quad \rightarrow (7.15)$$

KCL law at node 'B' is

$$V_A Y_2 - V_B (Y_2+Y_4) = V_o \frac{(Y_2+Y_4)}{A_o}$$

$$V_A = V_o \frac{(Y_2+Y_4)}{A_o Y_2}$$

$$\text{voltage gain} = \frac{V_o}{V_i} = \frac{A_o Y_1 Y_2}{Y_1 Y_2 + Y_4(Y_1+Y_2+Y_3) + Y_2 Y_3 (1-A_o)}$$



Second order low pass filter

Transfer function of low pass filter = H(S)

$$H(S) = \frac{A_o}{S^2C^2R^2 + SCR(3-A_o)+1} \rightarrow 7.18$$

$$H(S) = \frac{A_o \omega_h^2}{S^2 + \alpha\omega_h S + \omega_h^2} \rightarrow 7.19$$

where

A_o = gain

ω_h = upper cut off frequency in radian/second

α = damping coefficient

$$\omega_h = 1/RC \rightarrow 7.20$$

$$\alpha = (3 - A_o) \rightarrow 7.21$$

$$H(j\omega) = \frac{A_o}{(j\omega/\omega_h)^2 + j\alpha(\omega/\omega_h) + 1} \rightarrow 7.22$$

Normalized Expression for low Pass filter is

$$H(jw) = \frac{A_0}{S_n^2 + \alpha S_n + 1}$$

The expression & magnitude in dB & transfer function

$$20\log|H(jw)| = 20\log \frac{A_0}{\sqrt{\left(1-\frac{w^2}{w_h^2}\right)^2 + \left(\alpha\, w/w_h\right)^2}}$$